SWISS PHOTONICS

Scalable electro-optical packaging of silicon photonics components

Bert Jan Offrein

Swissphotonics workshop
Miniaturized Photonic Packaging

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Outline

- The need for integration at component and system level
  - CMOS silicon photonics with embedded III-V materials
  - High channel count silicon photonics packaging
- Summary

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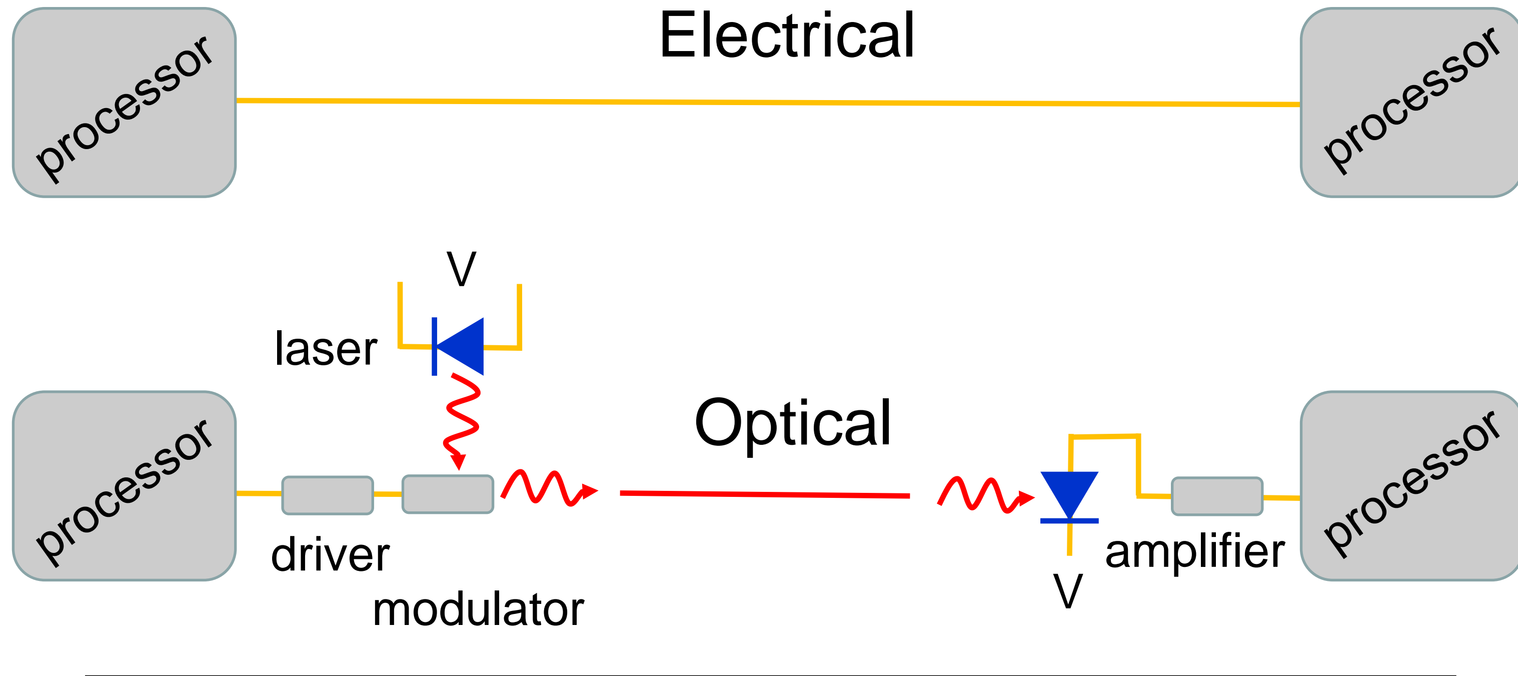
Communication between two processors



Optical communication:

- 1000 x Larger bandwidth
- 1000 x Lower loss
- 100 x Larger distance

Scalability & Power efficiency !!!

Optical communication requires many more components and assembly steps !!!

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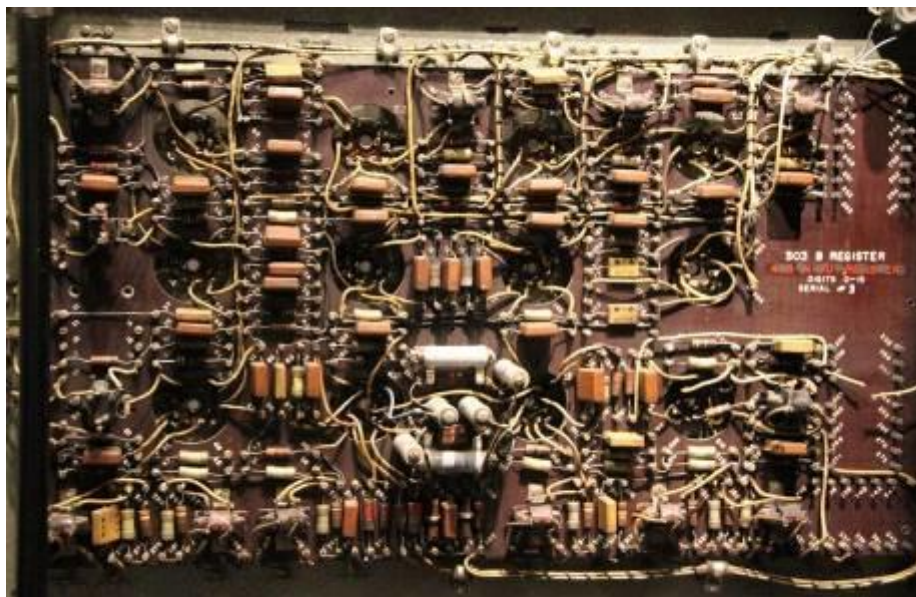
Why integration? Looking back, electronics

Pictures taken at:



Whirlwind, MIT, 1952

EAI 580 patch panel, Electronic Associates, 1968

Today's state of computing is based on:

- Integration and scaling of the logic functions (CMOS electronics)
- Integration and scaling of the interconnects (PCB technology & assembly)

For optical interconnects, this resembles:

- Electro-optical integration and scaling of transceiver technology
- Integration of optical connectivity and signal distribution

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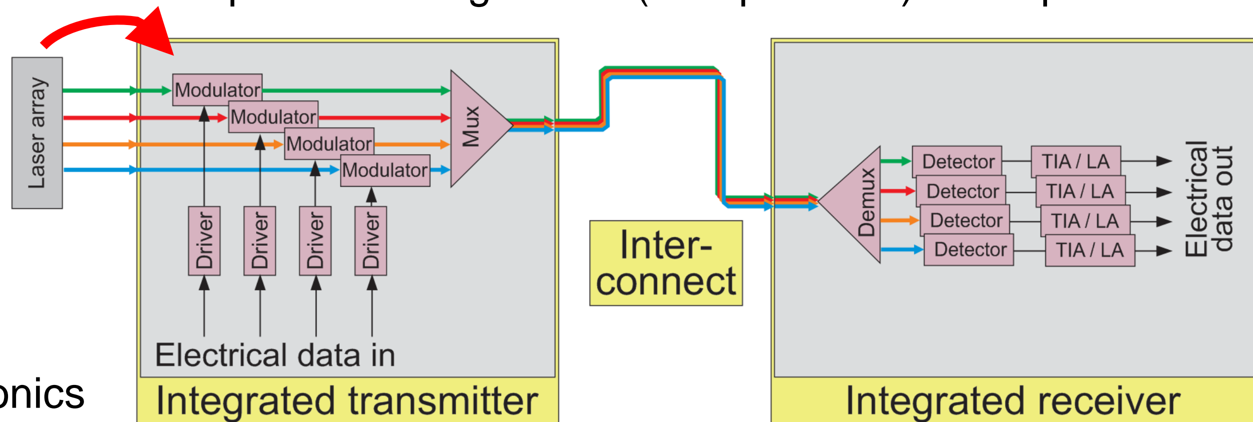
Photonics technologies for system-level integration

1 Chip-level: CMOS silicon photonics + Active photonics devices

- Si photonics provides all required buliding blocks (except lasers) on chip-level:

  - Modulators
  - Drivers
  - Detectors
  - Amplifiers
  - WDM filters

  + CMOS electronics



2 System-level: Scalable chip-to-fiber connectivity

- One step mating of numerous optical interfaces
- Provide electrical and optical signal routing capability
- Enable a simultaneous interfacing of electrical and optical connections

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Photonics technologies for system-level integration

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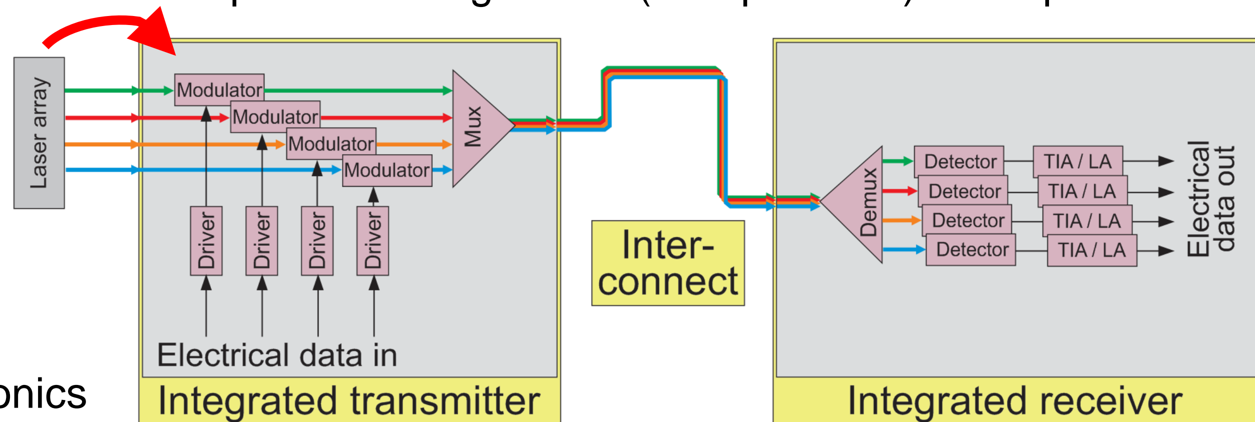

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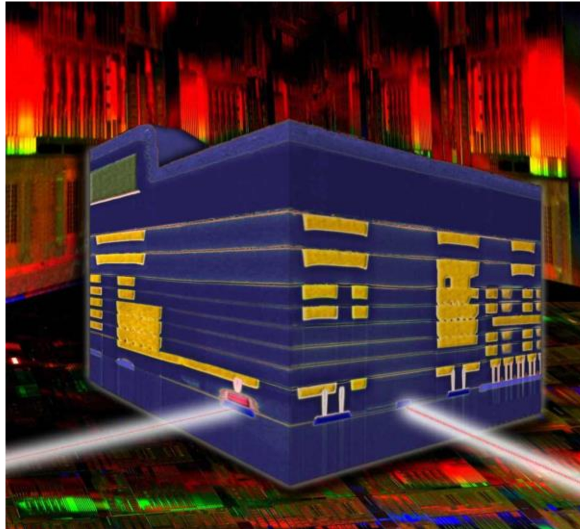
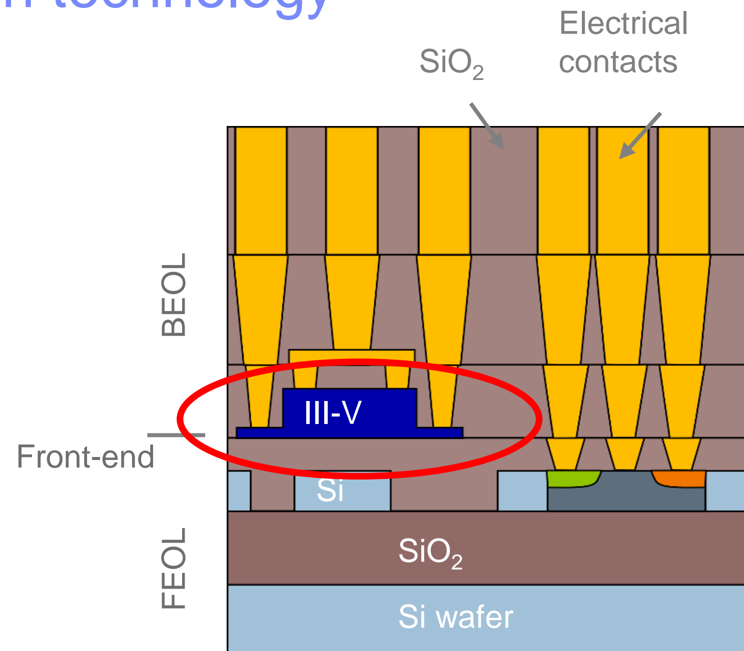
CMOS Embedded III-V on silicon technology



CMOS Si Photonics



… + III-V functionality

- Overcome discrete laser and assembly cost
- New functions, tightly combining electronics, passive and active photonics

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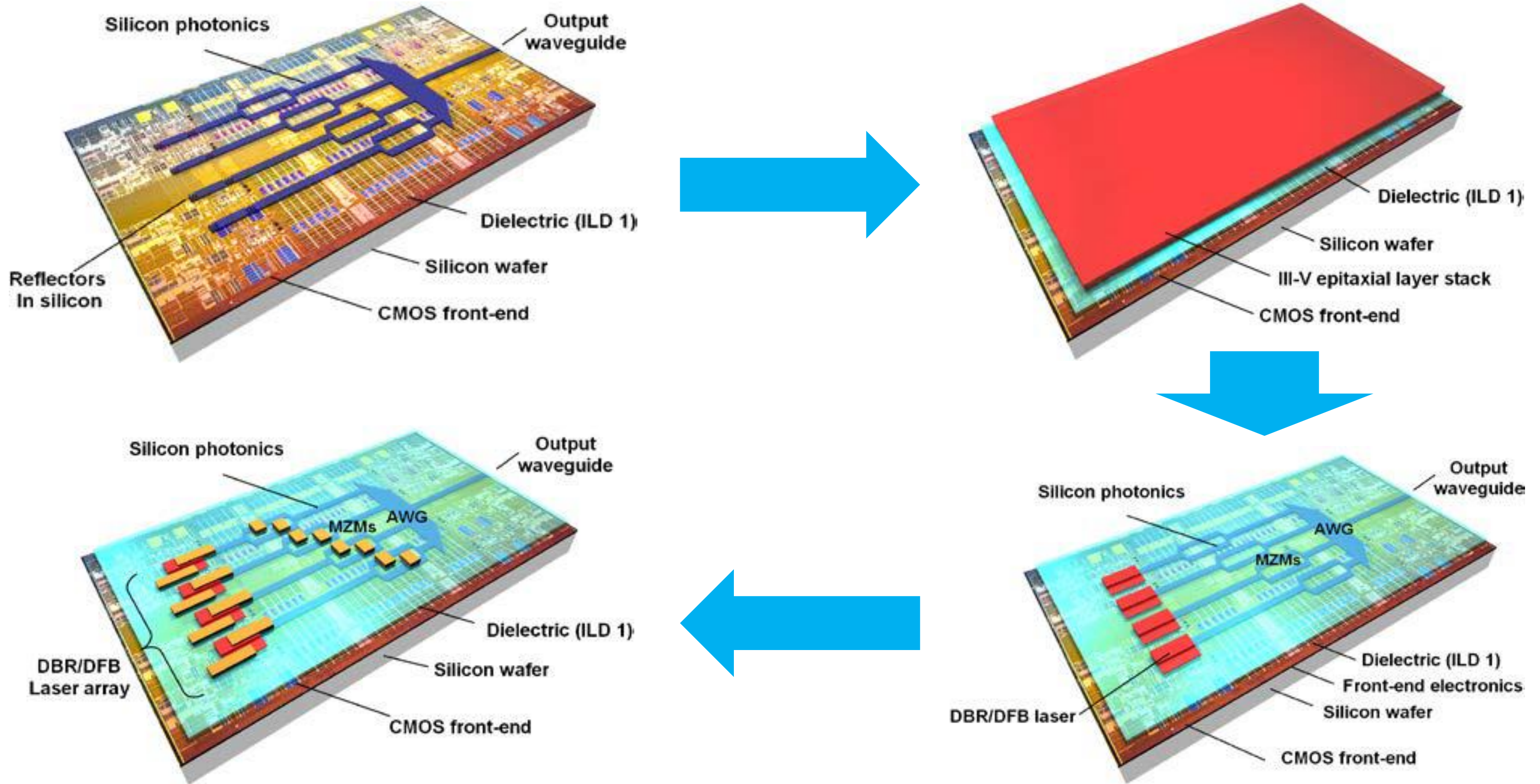
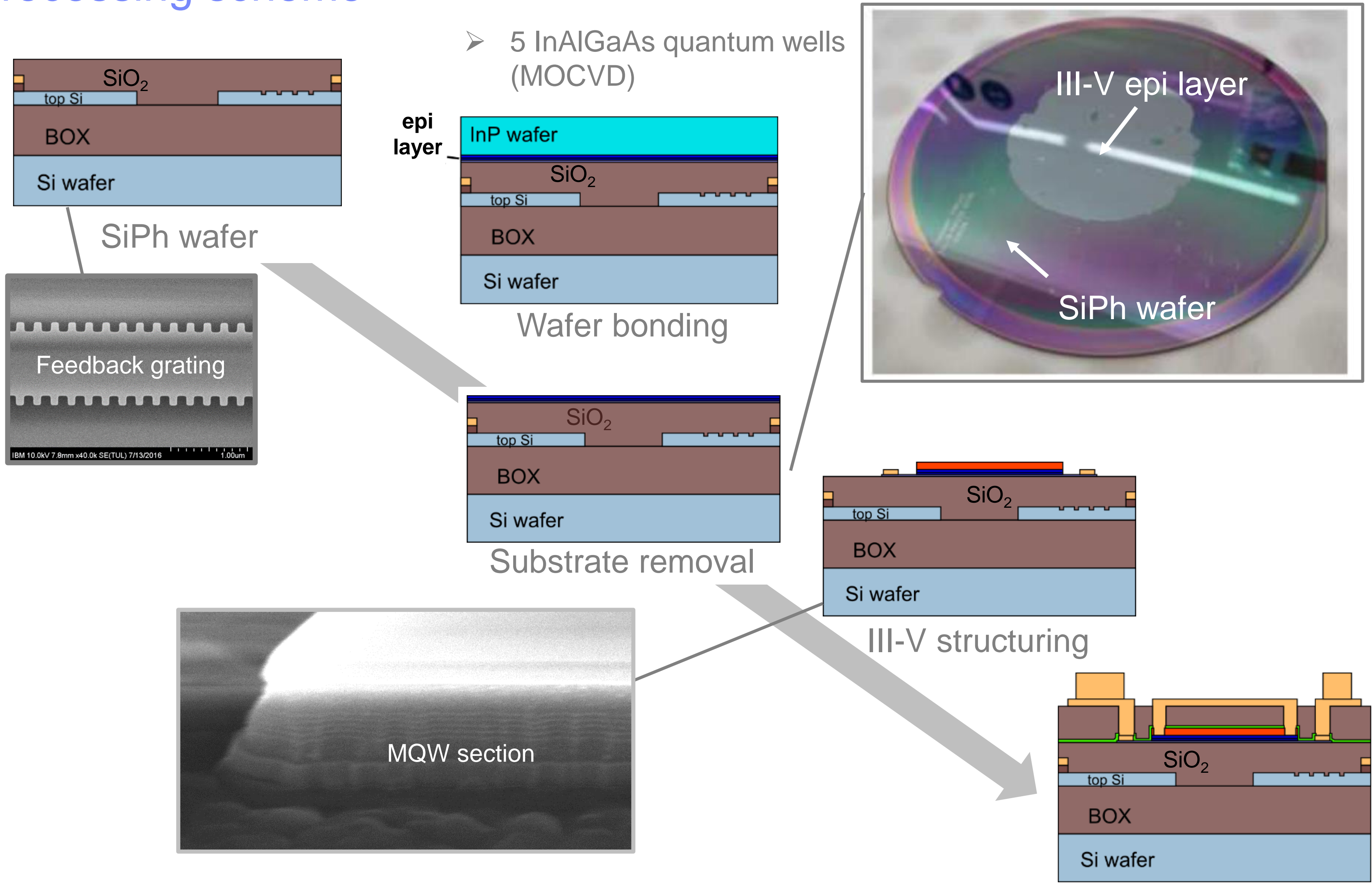
H2020 EU project DIMENSION



TECHNISCHE UNIVERSITÄT DRESDEN IBM ADVA Optical Networking ihp ATHENS INFORMATION TECHNOLOGY optocap

Processing scheme



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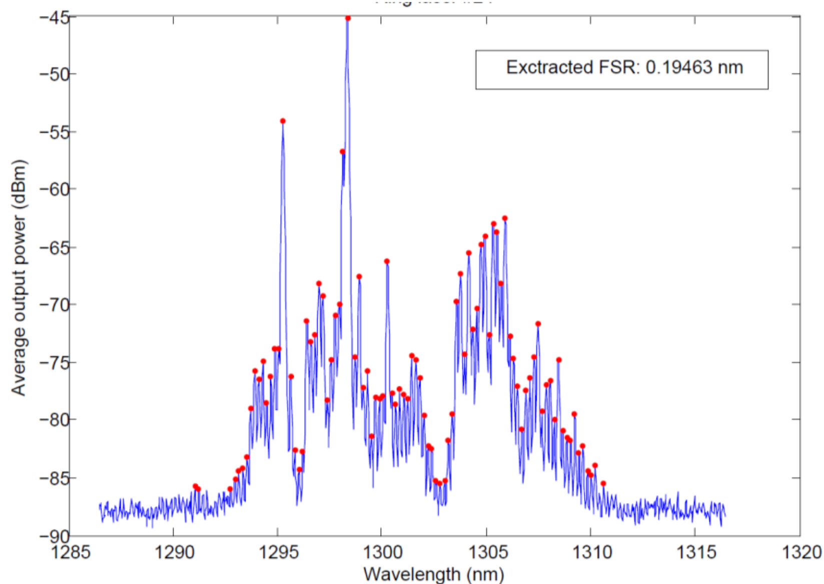
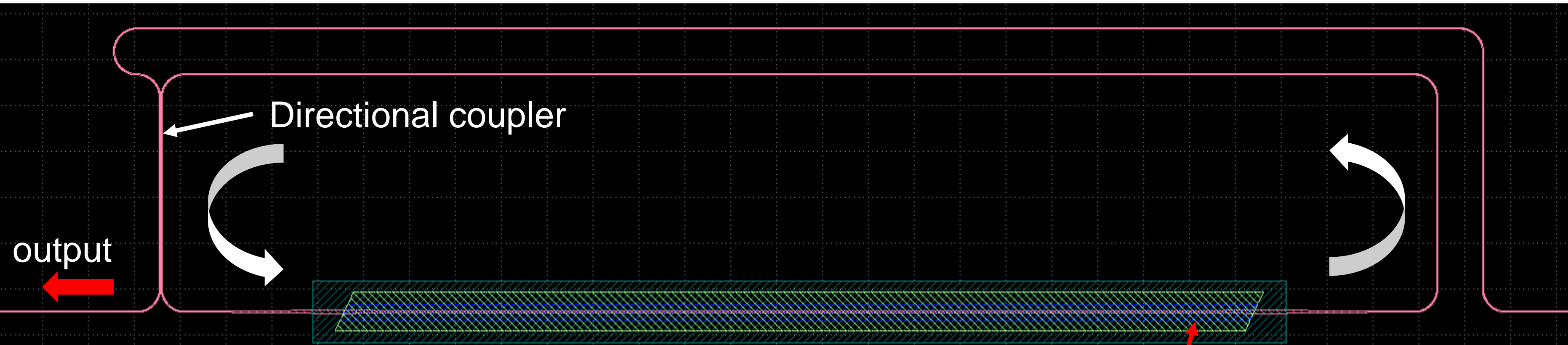
Optically pumped ring laser

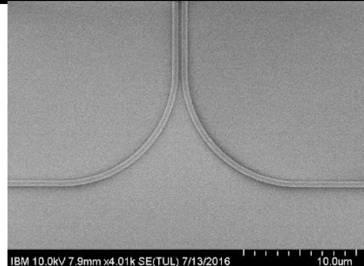


Measured FSR: 0.194 nm

Estimated FSR from ring: 0.203 nm
Estimated FSR from III-V: 0.266 nm

➢ Lasing with feedback from silicon photonics





Gain section

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Photonics technologies for system-level integration

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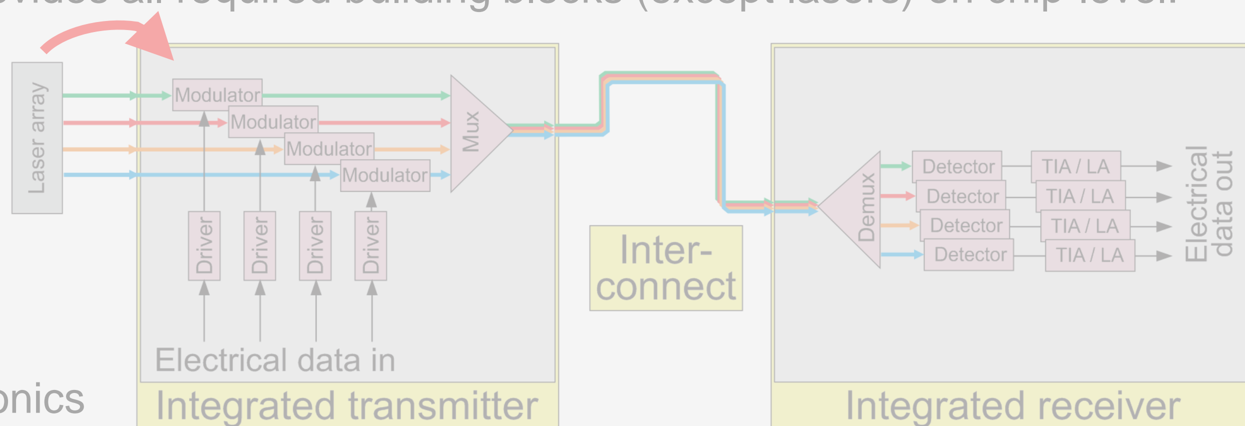

2 System-level: Scalable chip-to-fiber connectivity

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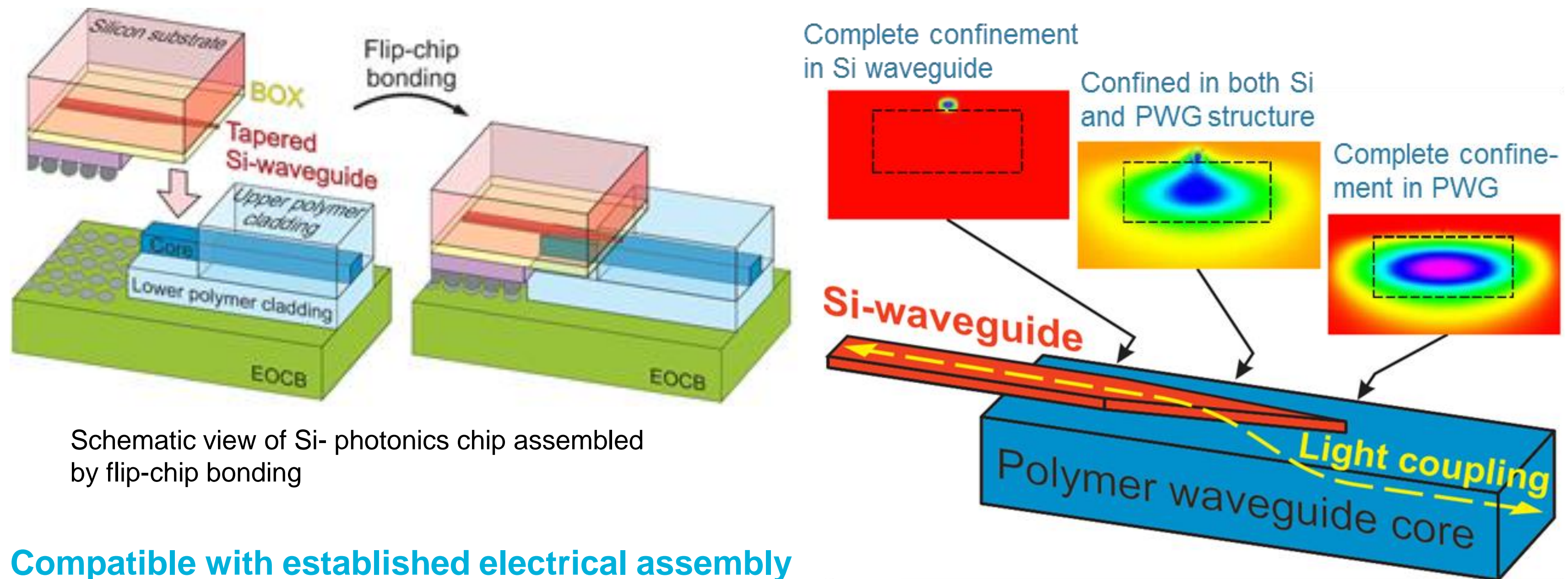
Adiabatic optical coupling using polymer waveguides

Principle:

– Contact between the silicon waveguide taper and the polymer waveguide (PWG), achieved by flip-chip bonding, enables adiabatic optical coupling



Schematic view of Si- photonics chip assembled by flip-chip bonding

- **Compatible with established electrical assembly**
- **Simultaneous E/O interfacing**
- **Scalable to many optical channels**

- J. Shu, et al. "Efficient coupler between chip-level and board-level optical waveguides." *Optics letters* 36.18 (2011): 3614-3616.
- I. M. Soganci, et al. "Flip-chip optical couplers with scalable I/O count for silicon photonics." *Optics express* 21.13 (2013): 16075-16085.
- T. Barwicz, et al. "Low-cost interfacing of fibers to nanophotonic waveguides: design for fabrication and assembly tolerances.", *Photonics Journal, IEEE* 6.4 (2014): 1-18.

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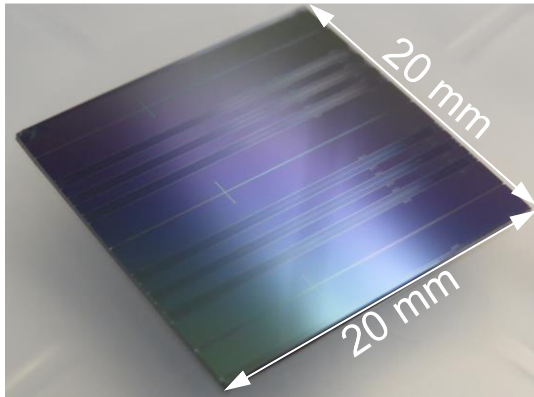
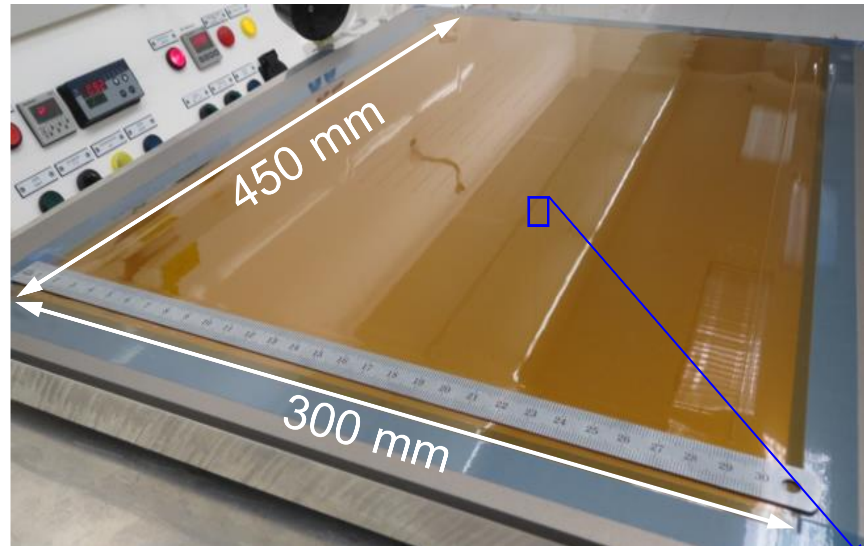
Single-mode polymer waveguide technology

SM polymer waveguides on **chips** (e.g. Si photonics chips)

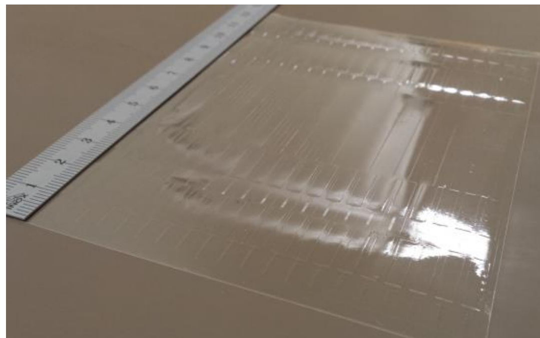


Chip-size

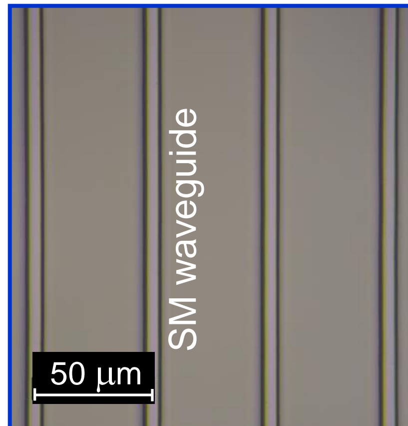
SM polymer waveguides on **panel-size flexible** substrates

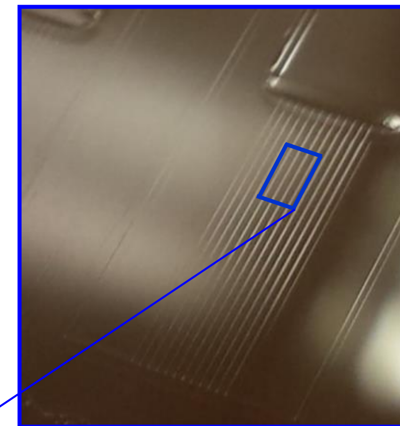


SM polymer waveguides on **wafer-size flexible** substrates



Wafer- size





Panel-size

R. Dangel, et al. Optics Express, 2015

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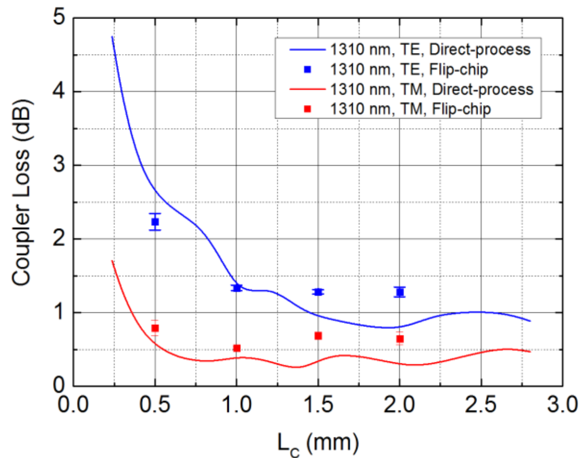
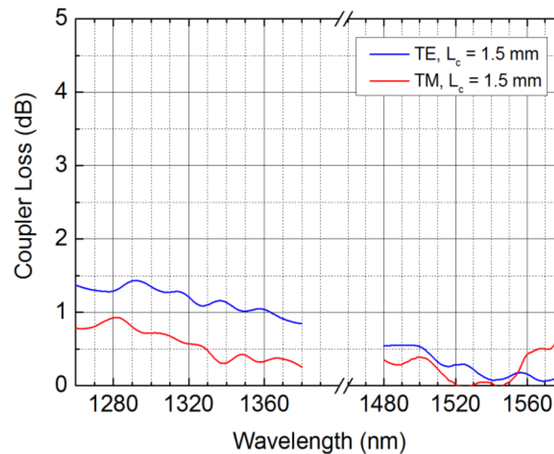
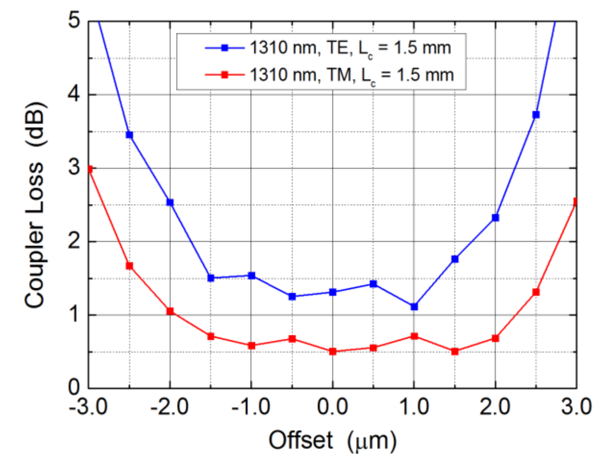
Adiabatic coupler loss characterization

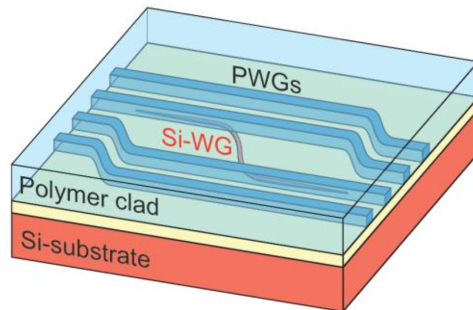
Coupler loss measurement:

- Direct-process vs Flip-chip bonding approach
- For $L_c \geq 1.0$ mm: Coupler loss < 1.5 dB, PDL ≤ 0.7 dB
- Operating in the O and C-band

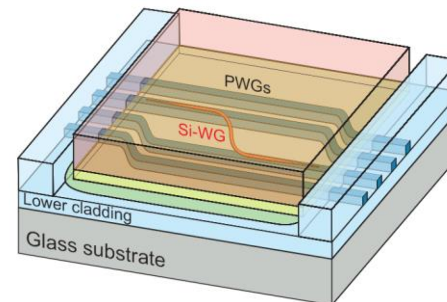








Polymer waveguides processed on chip



Polymer waveguides attached by flip-chip bonding

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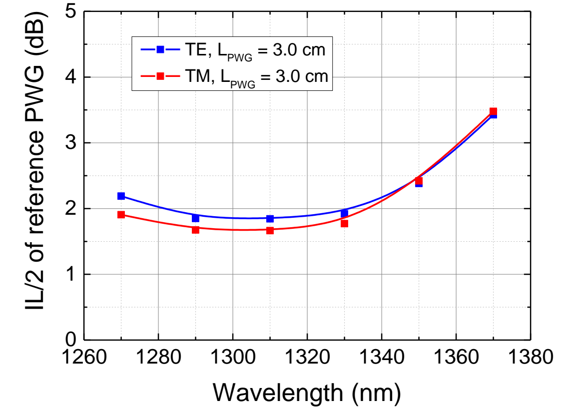
Insertion loss characterization (1)

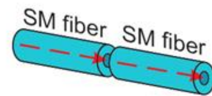
Insertion loss measurement:

- Wavelength sweep over O-band
  - Full path vs ref. PWG path
- Wavelength dependency mainly in the PWG



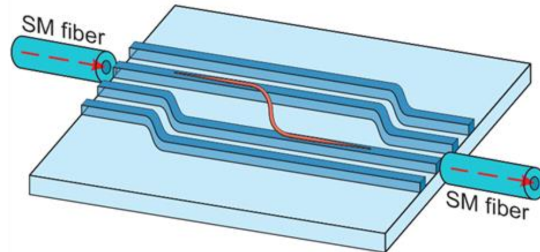
Insertion loss per 2 facets

Measurement ①

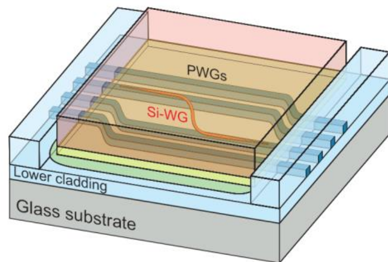


Fiber ➡ Fiber

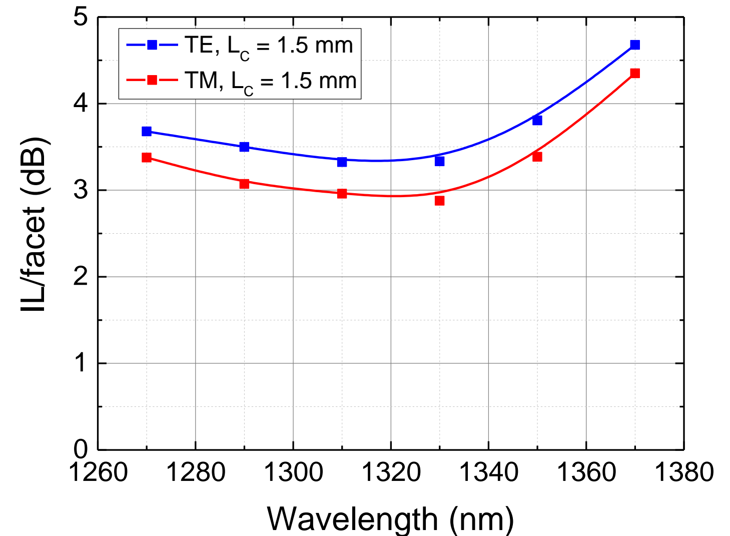
Measurement ②



Fiber ➡ PWG ➡ SiWG ➡ PWG ➡ Fiber



Schematic view of Si-photonics chip assembled by flip-chip bonding



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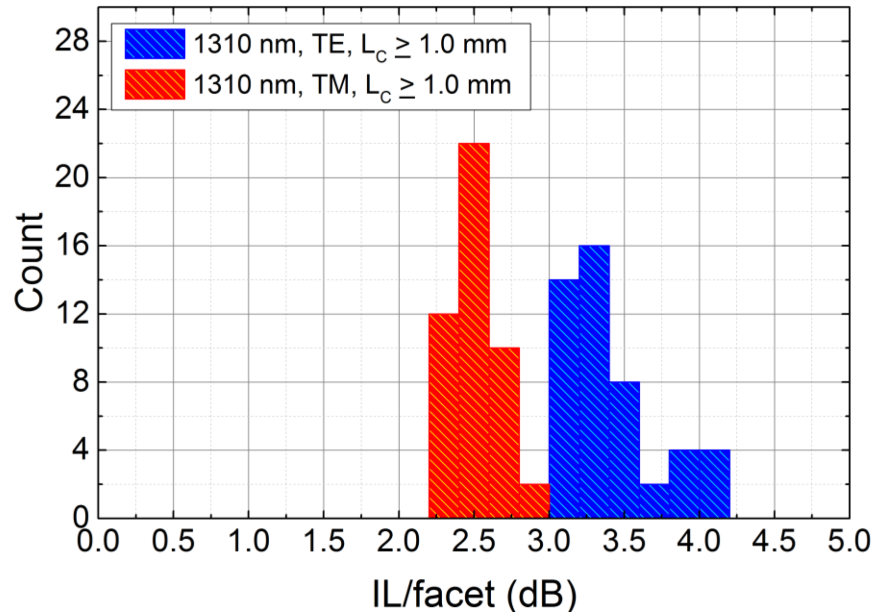
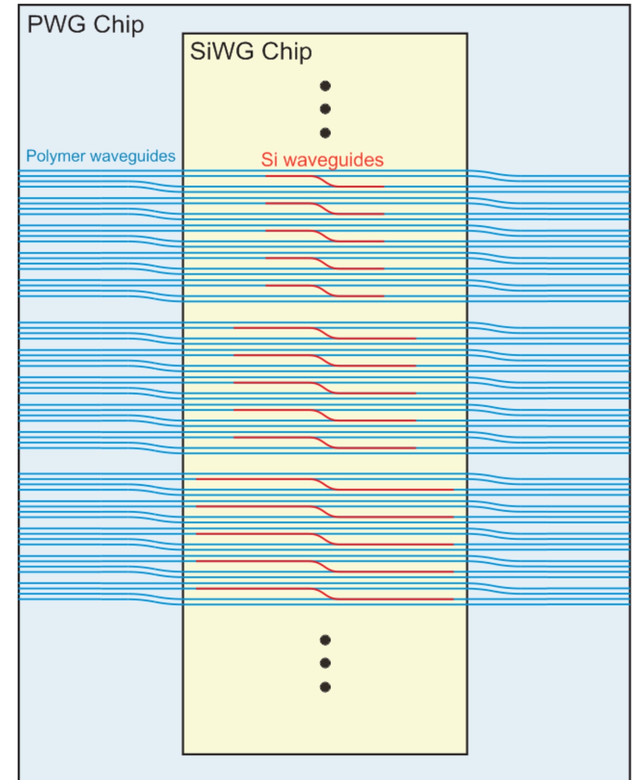
Insertion loss characterization (2)

Insertion loss statistics:

- High number of optical interfaces: **152** per chip
  - 94 interfaces for silicon couplers
  - 58 interfaces for polymer waveguide references
- For L_C = 0.5, 1.0 mm, …, 3.0 mm





Top-view of Si-photonics chip assembled by flip-chip bonding

~100 functional assembled optical IO's per chip

94 optical interfaces per chip, assembled simultaneously

- 17 connections used for offset measurements (34 interfaces)
- 30 connections for coupler length variations (60 interfaces)
- 24 (48 interfaces) from 25 connections plotted above, only one connection not functional

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Contract No 15.0313

Agreement No 688172

Contract No 15.0339

Agreement No 688544

Contract No 15.0346

Agreement No 688572

Contract No 15.0309

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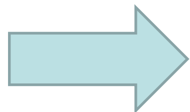
Summary

- **Miniaturized Photonic Packaging**
  - Chip level integration
    - CMOS+Passive+Active photonics
  - System-level integration
    - Adiabatic optical coupling as a scalable, efficient, broadband and polarization independent fiber-to-chip interfacing solution



Path towards high level of electro-optical integration & scalability

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