Software-defined Flash LiDAR

Smart next-generation sensing using system-on-chip detection processing

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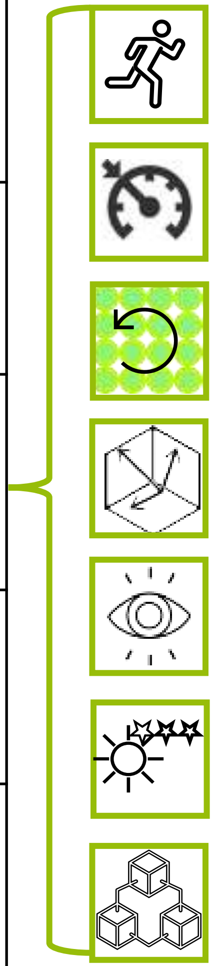
Fastree3D-System_on_Chip_LiDAR.pptx V.2

Outline

- Benefits of software-defined sensing
- CMOS single-photon detection evolution
- Flash LiDAR SoC approach and results
- Software-based detection performance improvement
  - Background light mitigation
  - Interference suppression
  - Illumination optimization
- CMOS stacked circuits for next-generation sensing
  - Software-defined sensing and edge processing
  - Development of firmware and hardware for research

Adapting 3D sensing to requirements

	Domain	Application	Illustration	Needs
Motion sensing latency requirement	**Transportation**	Collision avoidance, Localisation Traffic monitoring		
	Logistics	Localisation and path planning, collision avoidance		
	Manufacturing	Precision positioning and control, high safety		
	Safety	Variable perimeter control, people detection and counting, door control		
	Augmented vision	3D gesture tracking, AR/VR anchoring		

Software-defined SPAD-based LiDAR

Fast

Motion sensing for emergency collision avoidance

Lowest latency

Δt <10ms ⇔ ΔZ <30cm @ 50km/h

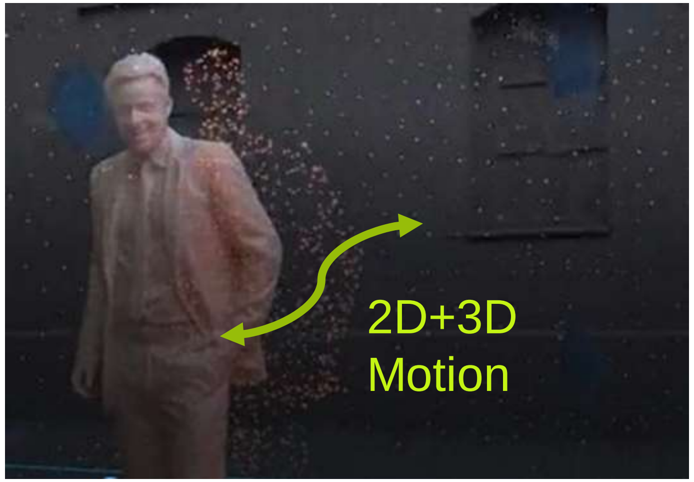
Safe

Low false detections under adverse lighting conditions

Quality control

Smart

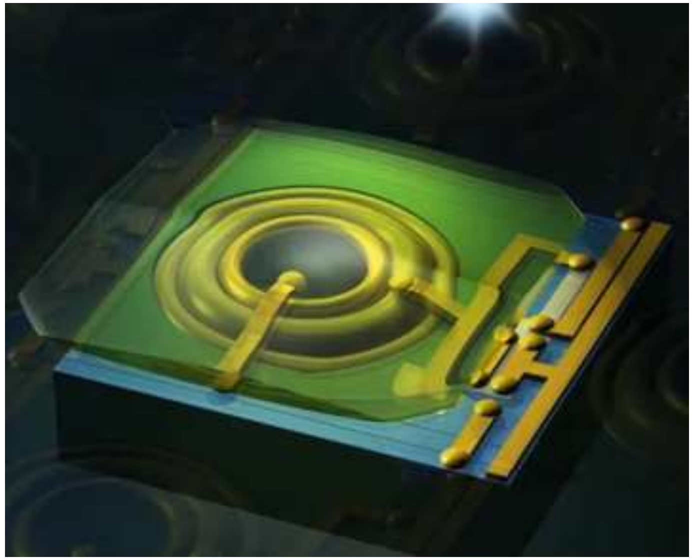
Realtime control and processing



Edge computing

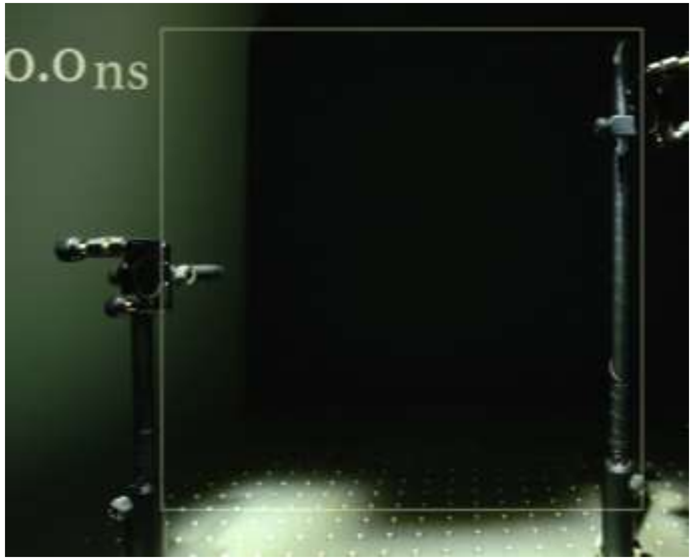
Single-photon detection processing

Single-photon avalanche diode sensitivity



Source : E. Charbon, EPFL aqua lab

Time-of-flight detection resolution + speed



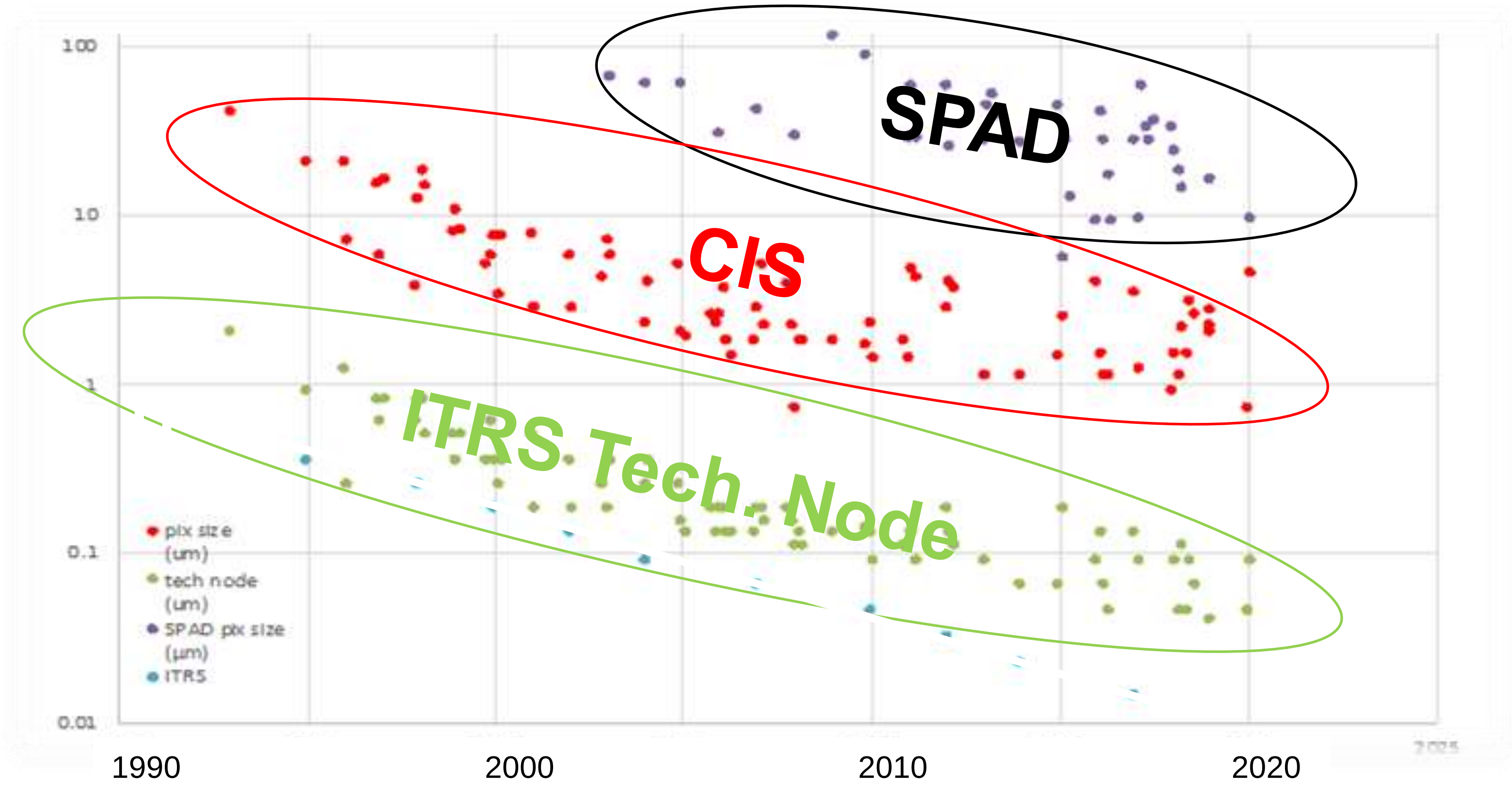
Source : D. Faccio, U. Glasgow

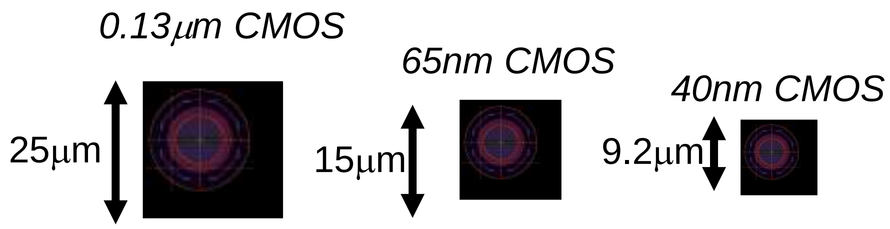
System on-chip requirements

- Fast read-out
  - ≈ 500 Mb/s for QQVGA (Detection x time x pixels)
- ToF accuracy / memory
  - TDC ≈ 100ps ⇔ Δ_Z ≈ 1.5cm
  - Memory for TCSPC histograms ⇒ 1.2 GB for QQVGA (non-optimized)
- Large 2D pixel count
  - Angular resolution : QQVGA @ 30° FoV ≈ 0.1°

Quarter-QVGA (QQVGA) resolution of 160 × 120 = 19'200 pixels

CMOS SPAD miniaturization trends





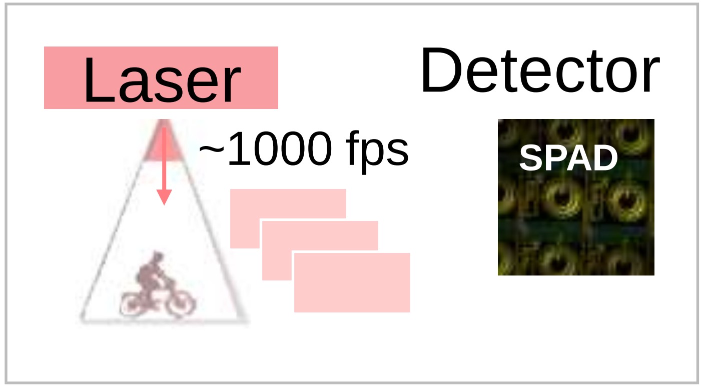
Source: Albert Theuwissen, Harald Homulle, Edoardo Charbon

- Evolution
  - Low pitch
  - High fill factor
  - 3D-IC for performance
- CIS trends +10 years
  - High voltage (older nodes support)
  - Guard rings
  - Lack of backside illumination process
  - Lower production volume

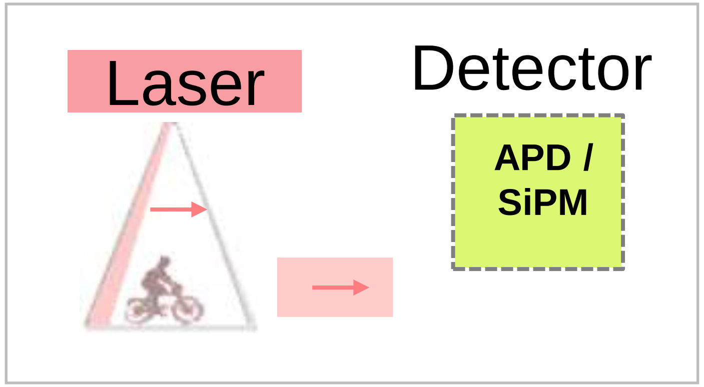
Flash LiDAR implementation principle

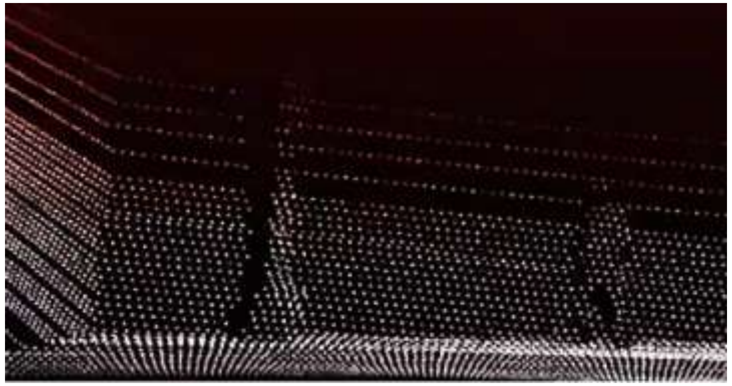
Animation

Flash



Scanner





Images acquired from the web for illustration only

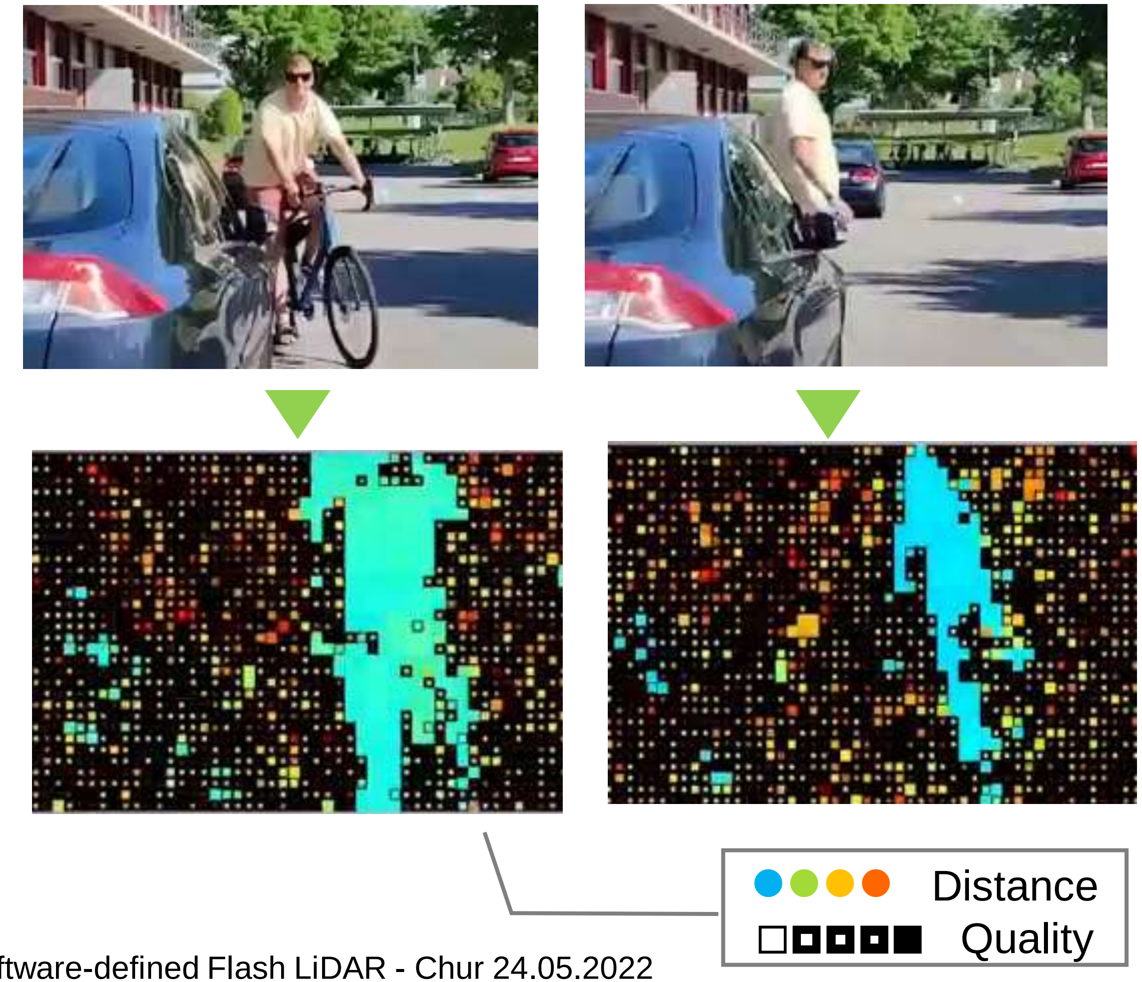
Flash

- Fast acquisition (MHz) of full 2D frame
- Optical power temporal distribution (high peak, low average)

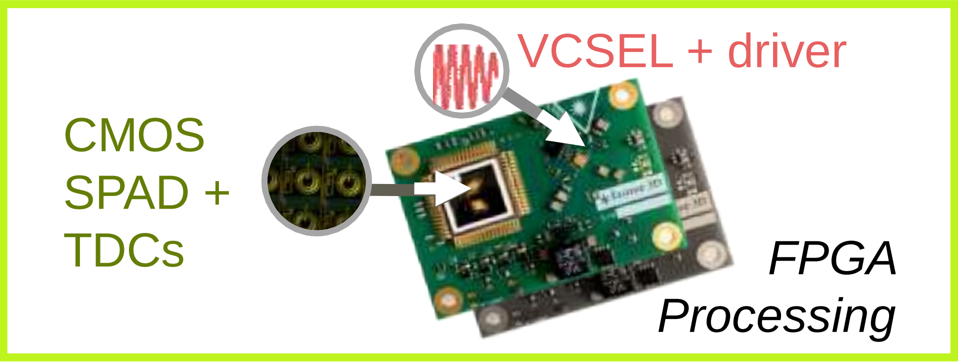
Digital processing

- Optimized ToF algorithms
- Signal to noise improvement

Flash LiDAR prototype evaluation

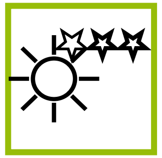


- ✓ Software-defined
- ✓ 2K pixels CMOS SPAD detector
- ✓ Flash illumination (VCSEL)
- ✓ Range 30m @ 10%r, 60klux



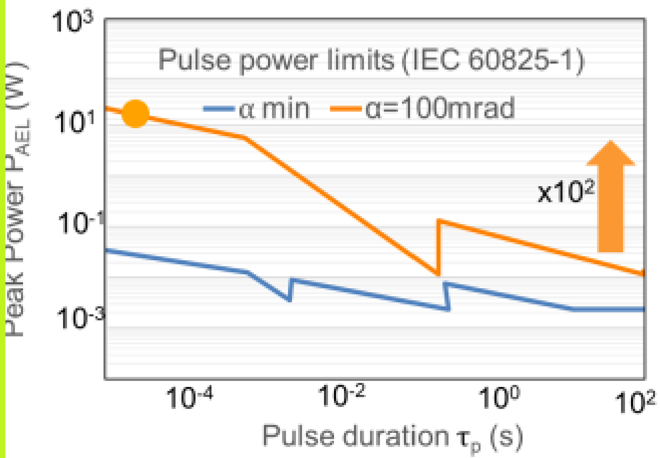
Software optimization advances

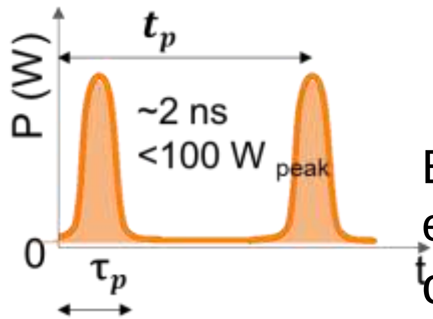
Illumination to 30-50m



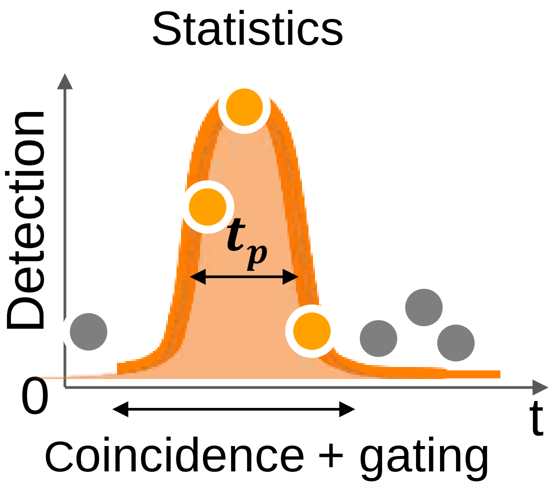
Sunlight removal

Interference removal

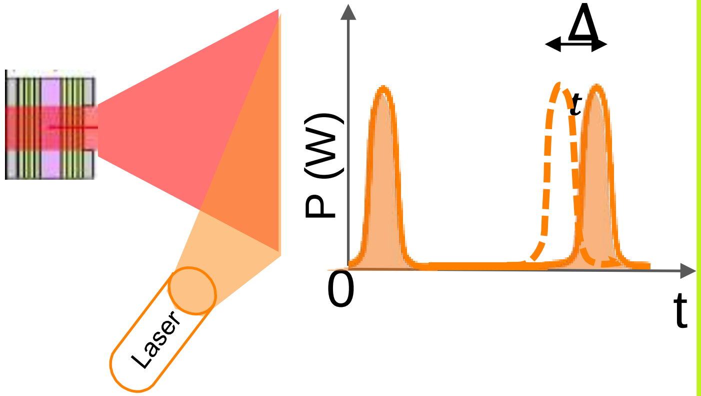




Eye-safe emission control



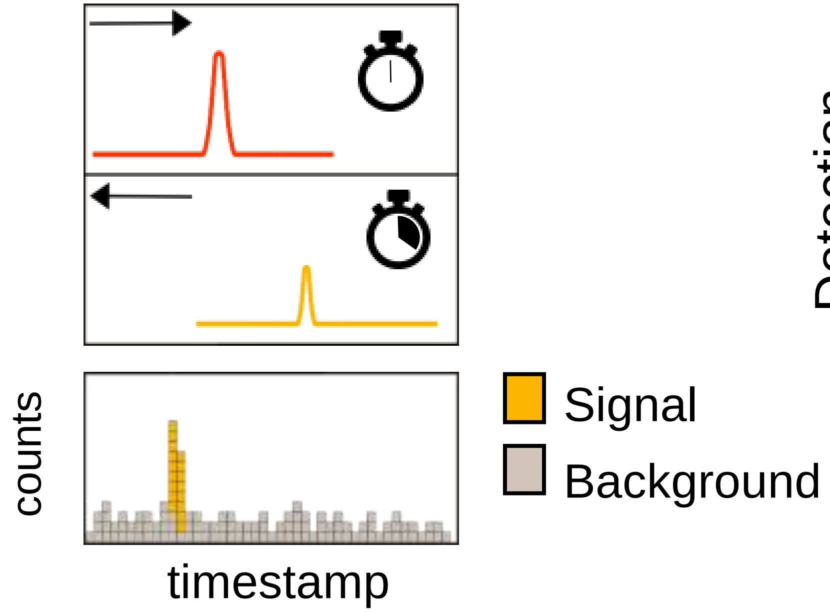
- Coincidence photon
- Noise photon (sunlight)



- Delay coding
- Decorrelation Tx/Rx
- SNBR > 35dB

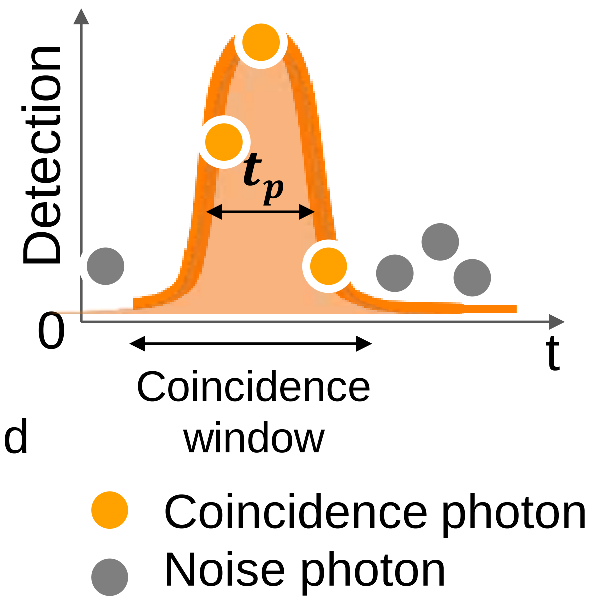
Software-defined background light mitigation

Time-stamp statistics



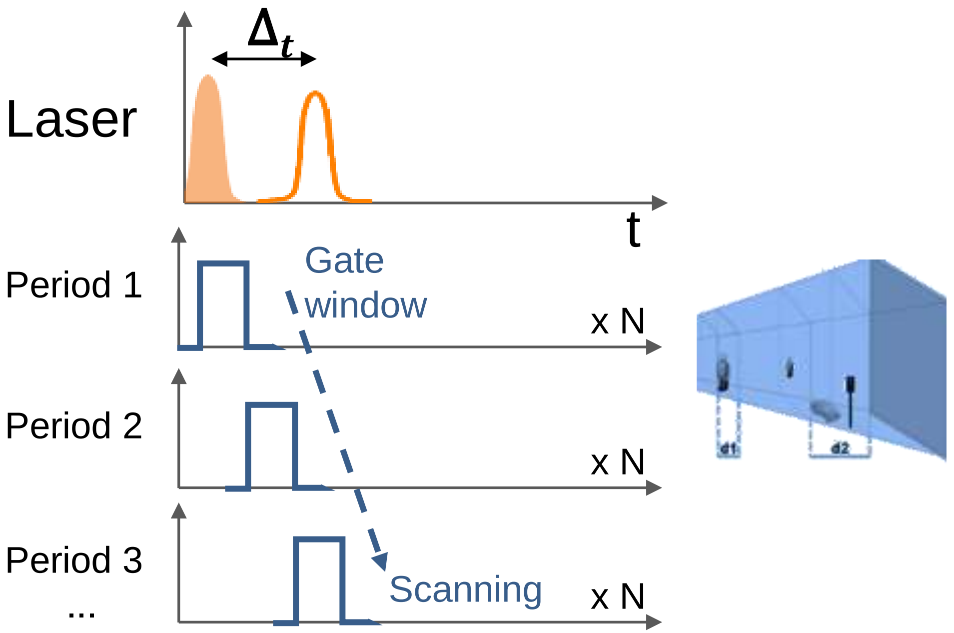
- Time Correlated Single Photon Counting (TCSPC)
- Optimized algorithms

Coincidence detection



- Multiple SPAD pixel (4-9)
- Coincidence control (t_{cw} 500ps-2ns)

Time-gating



- SPAD pixel gating
- Adaptive gating to range

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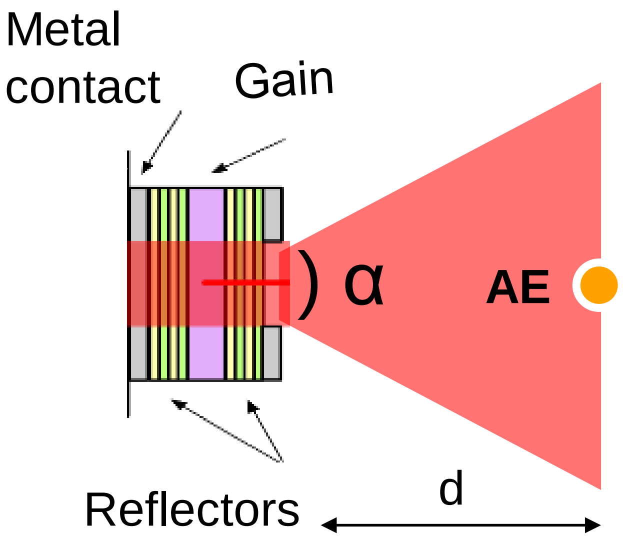
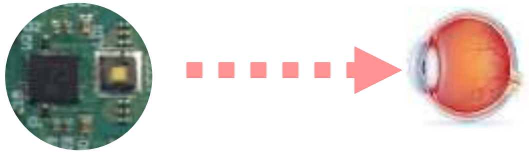
Software-defined illumination optimization

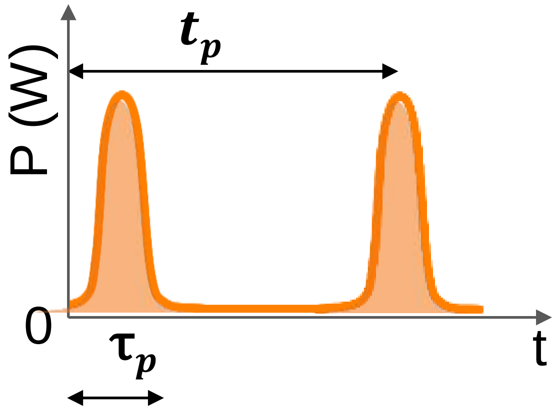
VCSEL Fast Pulses



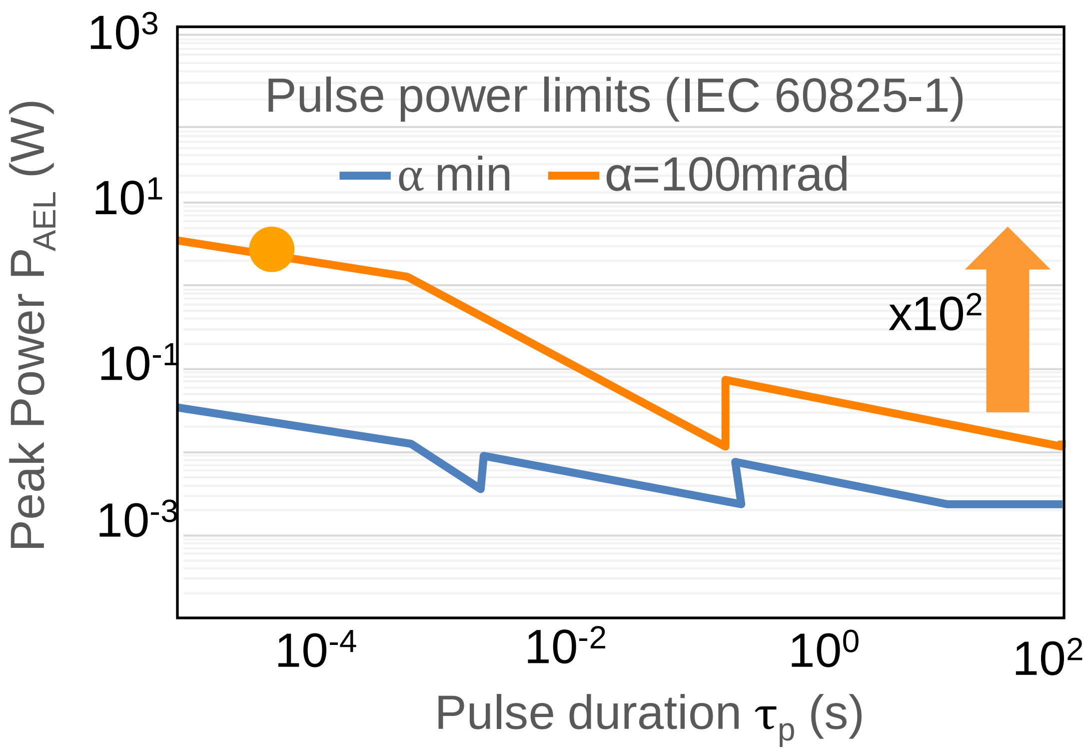
AEL: Accessible Emission Limit



High Peak Power



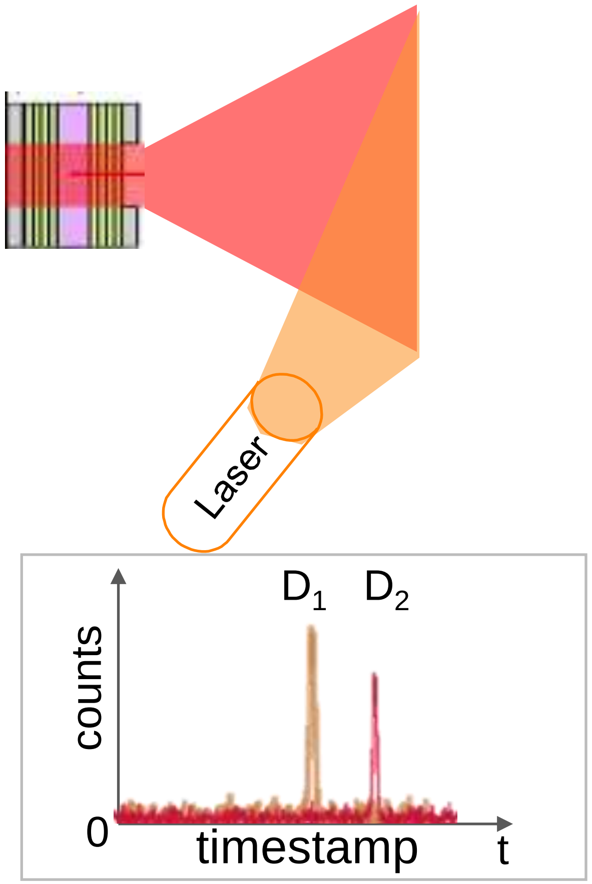
Eye-safety adjustment



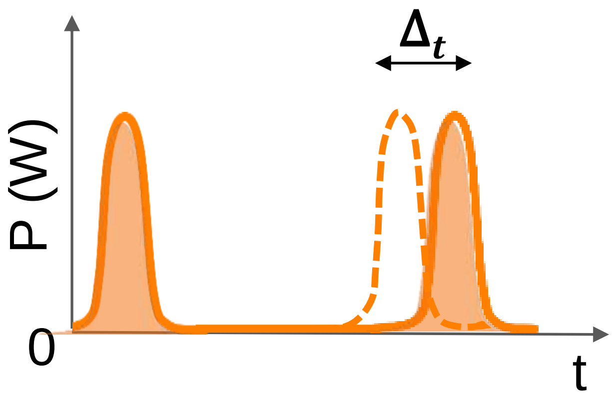
[1] S. T. Keller, F. Matteini, B. Penlae, and L. Carrara, “Novel illumination strategy for lidar enabled by update in the laser product standards,” J. Laser Appl., vol. 30, no. April, pp. 1–7, 2018.
[2] IEC 60825-1 : Safety of Laser Products—Part 1: Equipment Classification and Requirements, 3rd ed. (IEC, Geneva, 2014)

Software-defined interference suppression

Flash interference

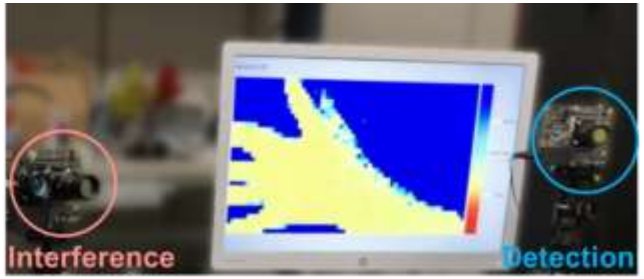


Pulse coding

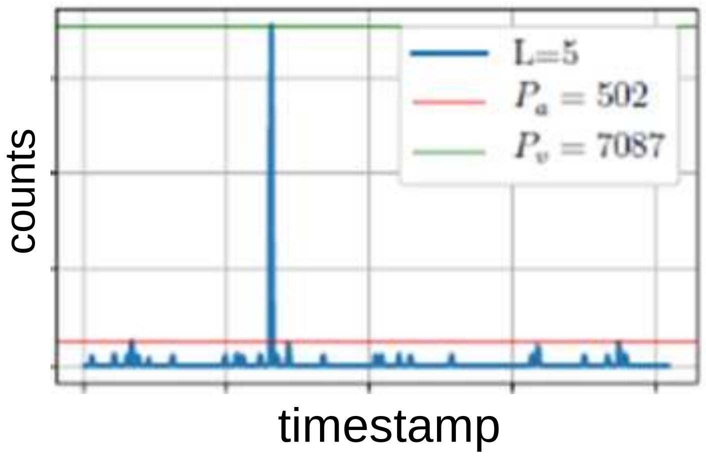


- Discrete random delays of the VCSEL laser pulses (3-5 bits)

Interference suppression

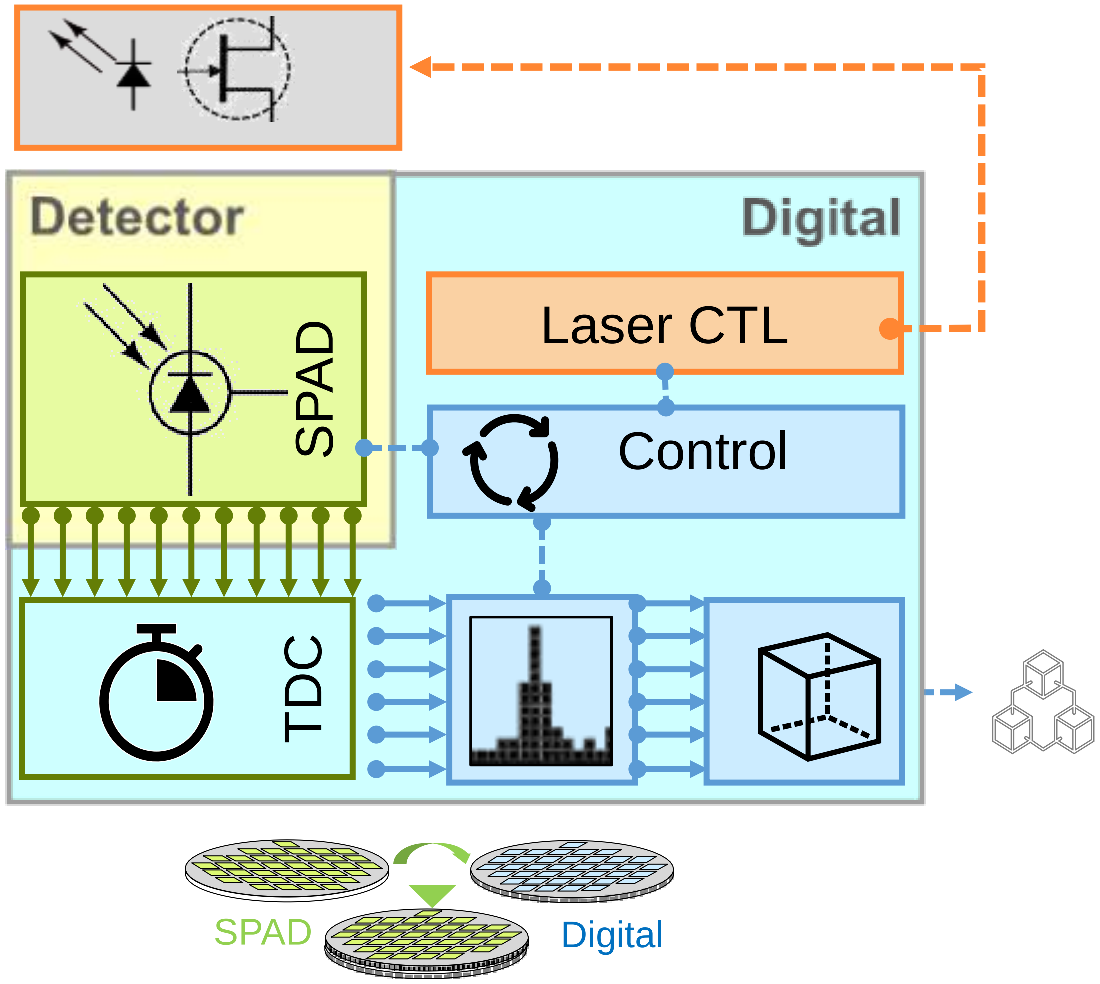


- Decorrelation Tx/Rx
- Signal / Noise ratio > 35dB



L. Carrara and A. Fiergolski, "An optical interference suppression scheme for TCSPC flash LiDAR imagers," Appl. Sci., vol. 9, no. 2206, pp. 1–15, 2019.

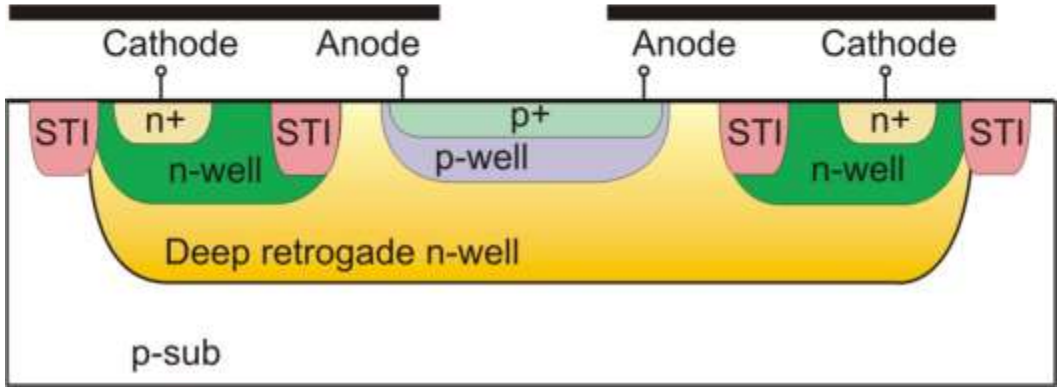
SoC implementation with 3D-IC



- High-resolution detection
  - Lower pitch size <7µm
  - Detection efficiency, gain > 10^6
  - 256 x 64-256 x 4 SPADs
  - Global shutter
- Hybrid Cu-Cu wafer bonding
- Digital processing & control
  - Time-gating
  - Coincidence for sunlight suppression
  - ToF processing
  - Adaptive illumination and RoI
  - Lower cost / pixel

From monolithic to 3D-IC stacked circuits

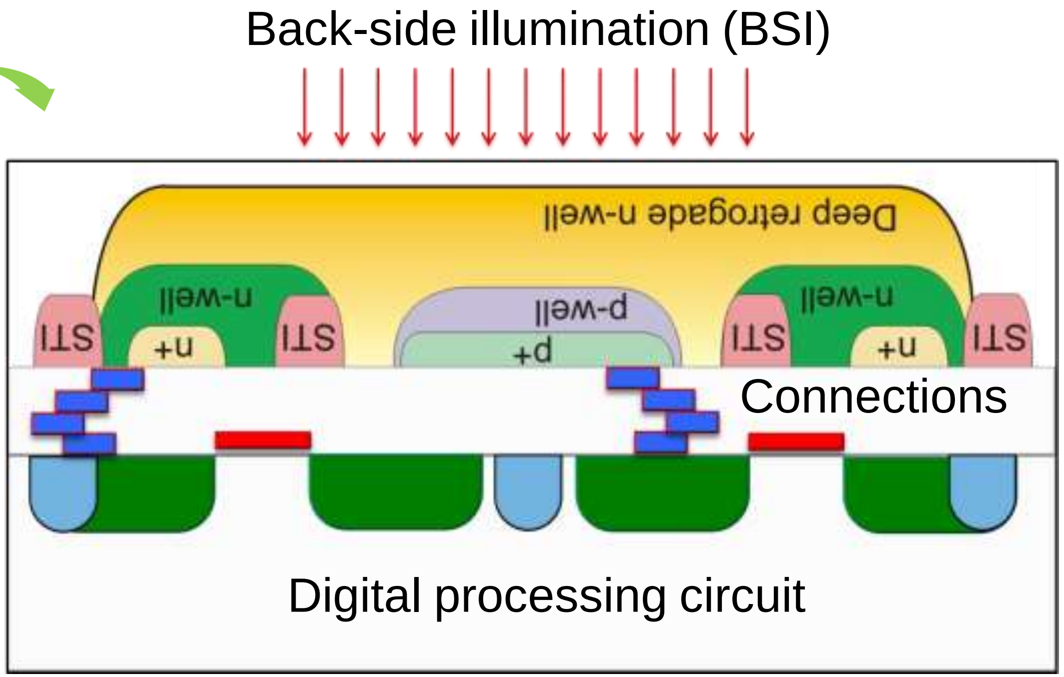
Monolithic implementations



- ✓ Simple electronics
- ✓ Lower costs

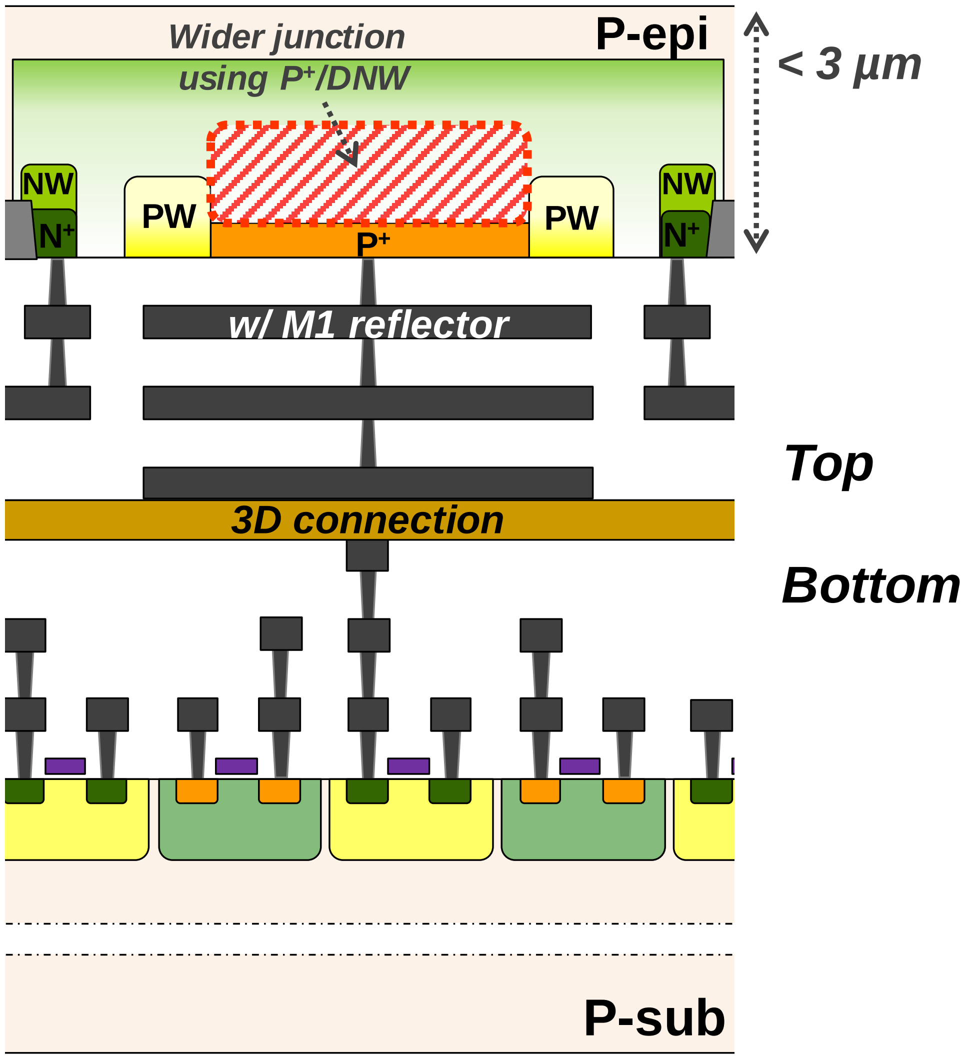
Sources : David Stoppa, Richard Henderson (schamatics)

3D-stacking at wafer level

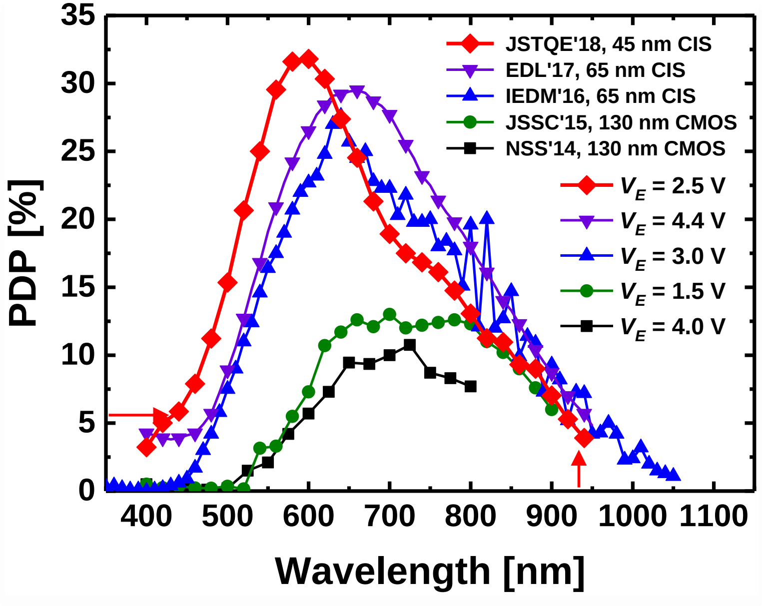


- ✓ Fill factor increase → sensitivity improvement
- ✓ Smaller pitch → higher pixel count
- ✓ Optimized CMOS for electronics → performance

3D wafer-level stacking evolution



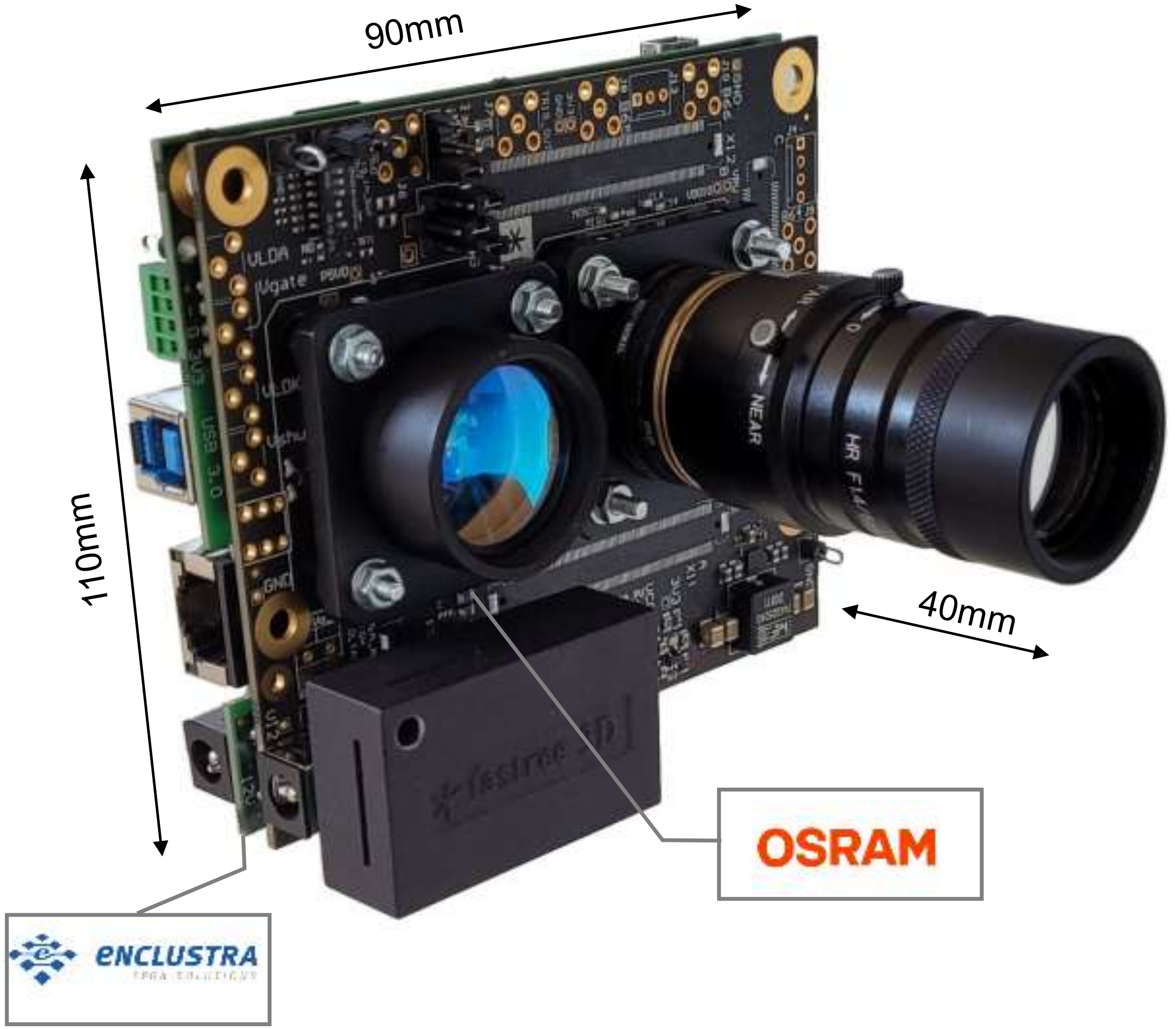
- SPADs (TSMC 65nm)
- TSV-less connections



- Electronic circuits (TSMC 45nm)
  - Quenching & recharge
  - Masking, region of interest
  - TDC (low power coupled oscillators)
  - Digital processing, coincidence management

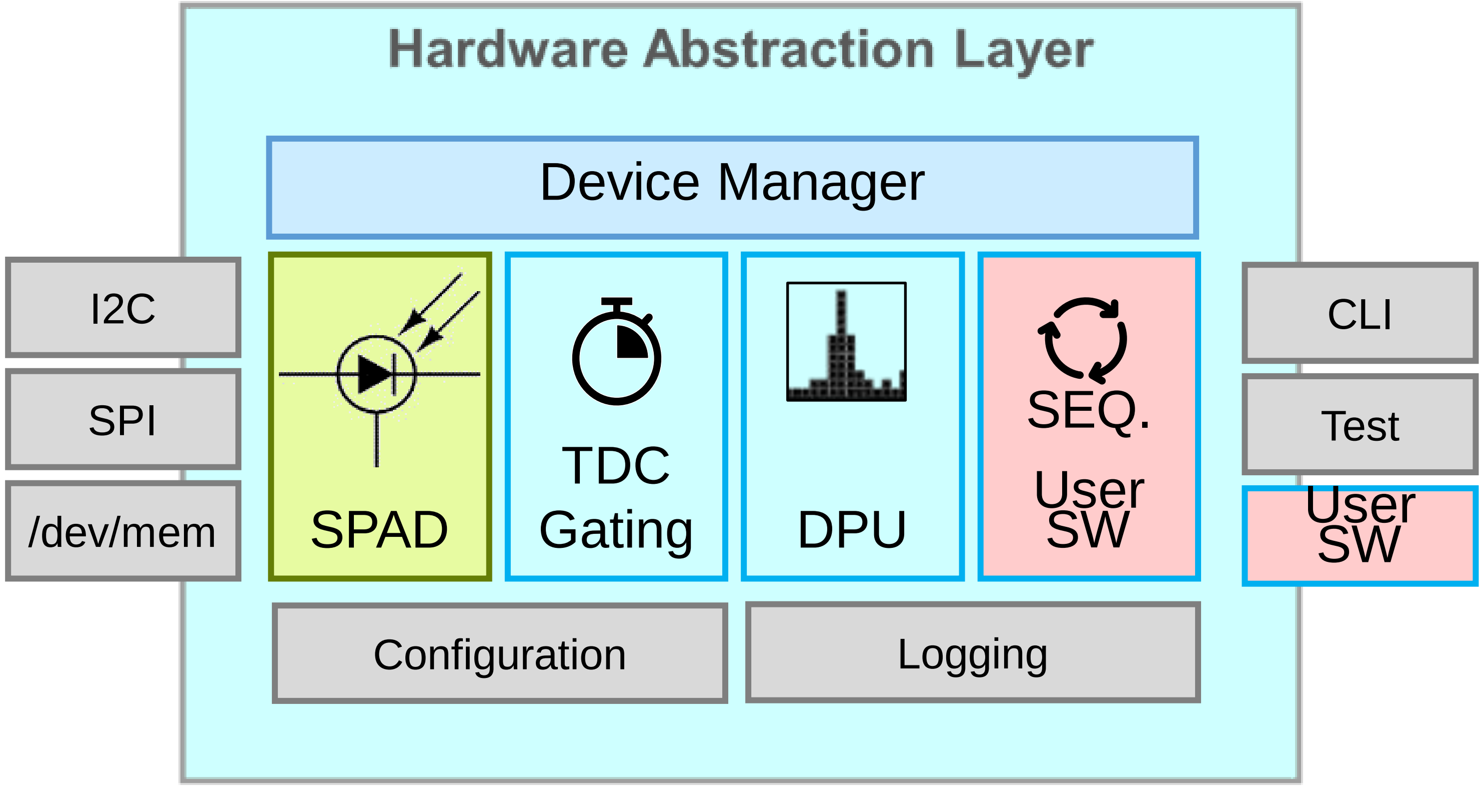
Sources : EPFL - A. Ximenes, P. Padmanabhan, ISSCC18, M.-J. Lee & Charbon, JSTQE18 + ., Jpn. J. Appl. Phys'18, P. Padmanabhan, ISSCC21

Development kit for R&D projects



- Sensor board
  - C1004 detector 60 x 32 pixels,
    - >30 fps Global shutter, 1.2 MB/s
  - Emitter
    - Driver, VCSEL array , illumination control
    - Optics (20-40° FoV tested)
- Processing : Xilinx's Zynq UltraScale
  - ARM Cortex-A53 + Cortex-R5 + Mali-400 GPU
  - FPGA fabric.
- Host board
  - Ethernet RJ45 (Automotive TE-1401-1 converter *1000Base-T GB IEEE802.3)
  - CAN, USB 2.0/3.0
  - Synchronisation : PTP (IEEE 1588)

Software-defined architecture



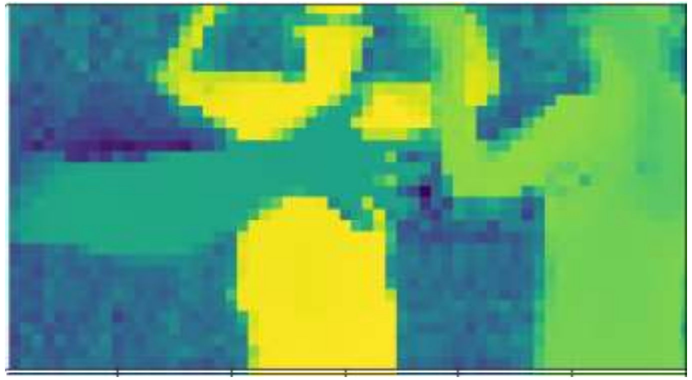
- Sensor acquisition software
- Hardware abstraction layer controls functions as C, C++, Python objects,
- Detector specific configuration and operation parameters,
- User-defined software in sequencer

Reference : A. Fiergolski. "A Multi-chip Data Acquisition System Based on a Heterogeneous System-on-Chip Platform". In: Proceedings of International Conference on Technology and Instrumentation in Particle Physics 2017. Ed. by Z.-A. Liu. Singapore: Springer Singapore, 2018, pp. 303–308. / Peary Software Repository. URL: https://gitlab.cern.ch/Caribou/peary

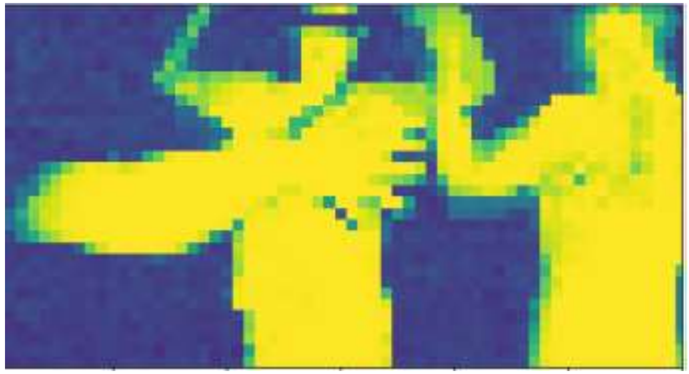
Software-defined 2D/3D edge-processing

(HDK screen dumps, roadmap or demo project)

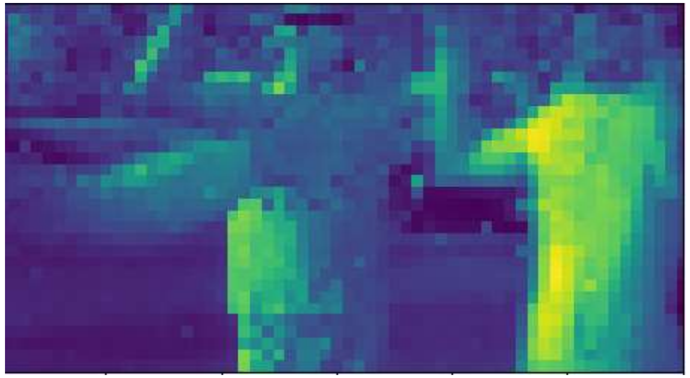
Distance point cloud

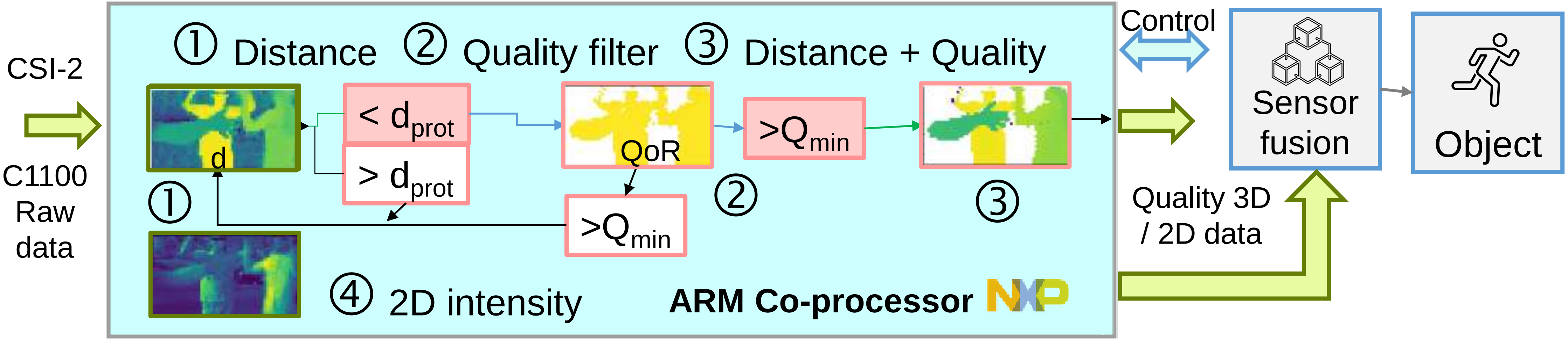


Quality control



Intensity image





*R&D acquisition on HDK Falcon, 30fps 60x32=2K pixels, short range 20m, 18° FoV optics, >10 klux * with 4W @30V , taken 2021-04*
(potential non-validated roadmap ~ 30m @ 4W/80V and 50M with 10W laser)

Thank you

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Automotive safety

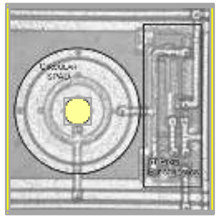
Autonomous vehicles

Fastree3D / EPFL collaboration history

ISSCC **2005**

Cristiano Niclass

59µm



SPIE **2014**

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Samuel Burri,
256 px LinoSPAD

ISSCC **2020**

7µm

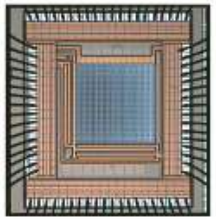
256x128 px
+ Coincidence
Preethi Padmanabhan

2022

fastree 3D

Adrian Fiergolski
2Kpx Falcon

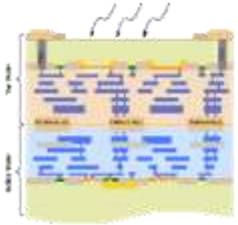
① CMOS SPAD ② World 1st miniaturization ③ World performance



Lucio Carrara

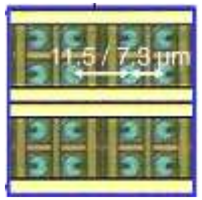
ISSCC **2009**

19µm / 3D IC



2018 Augusto Ximenes

9.4µm cells



Optica **2021**

1024 x1000 px
(9.4µm) 1000fps

4D imaging

** ISSCC is the "Olympics of Semiconductor industry", SPIE is the lworld's #1 photonics association*

EPFL aqua lab, R. Charbon 2021

EPFL

fastree 3D