VCSELs

Key components for optical interconnects

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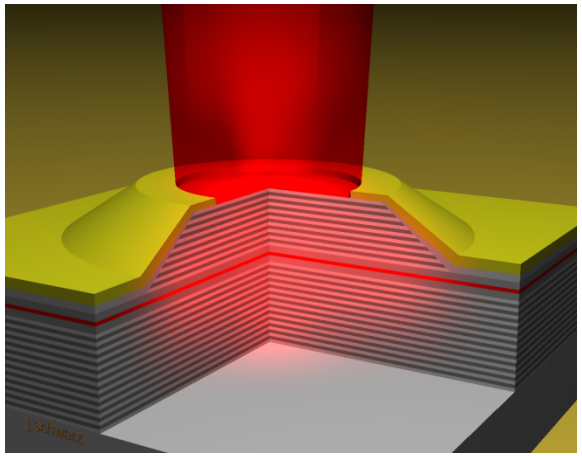
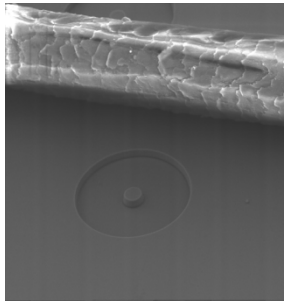
Outline

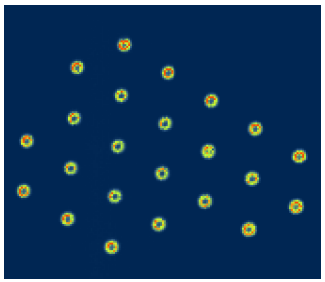
1. Overview
   - Key VCSEL properties and current VCSEL markets
2. 1999 projections for VCSEL based optical interconnects
   - 1999 technology roadmap for VCSELs
   - Fundamental limits
3. 10 G VCSELs
   - Electro-optical properties
   - Reliability
4. Optical USB: Mass fabrication of VCSELs
   - Producing more
   - Costing less
5. Summary

Key Properties

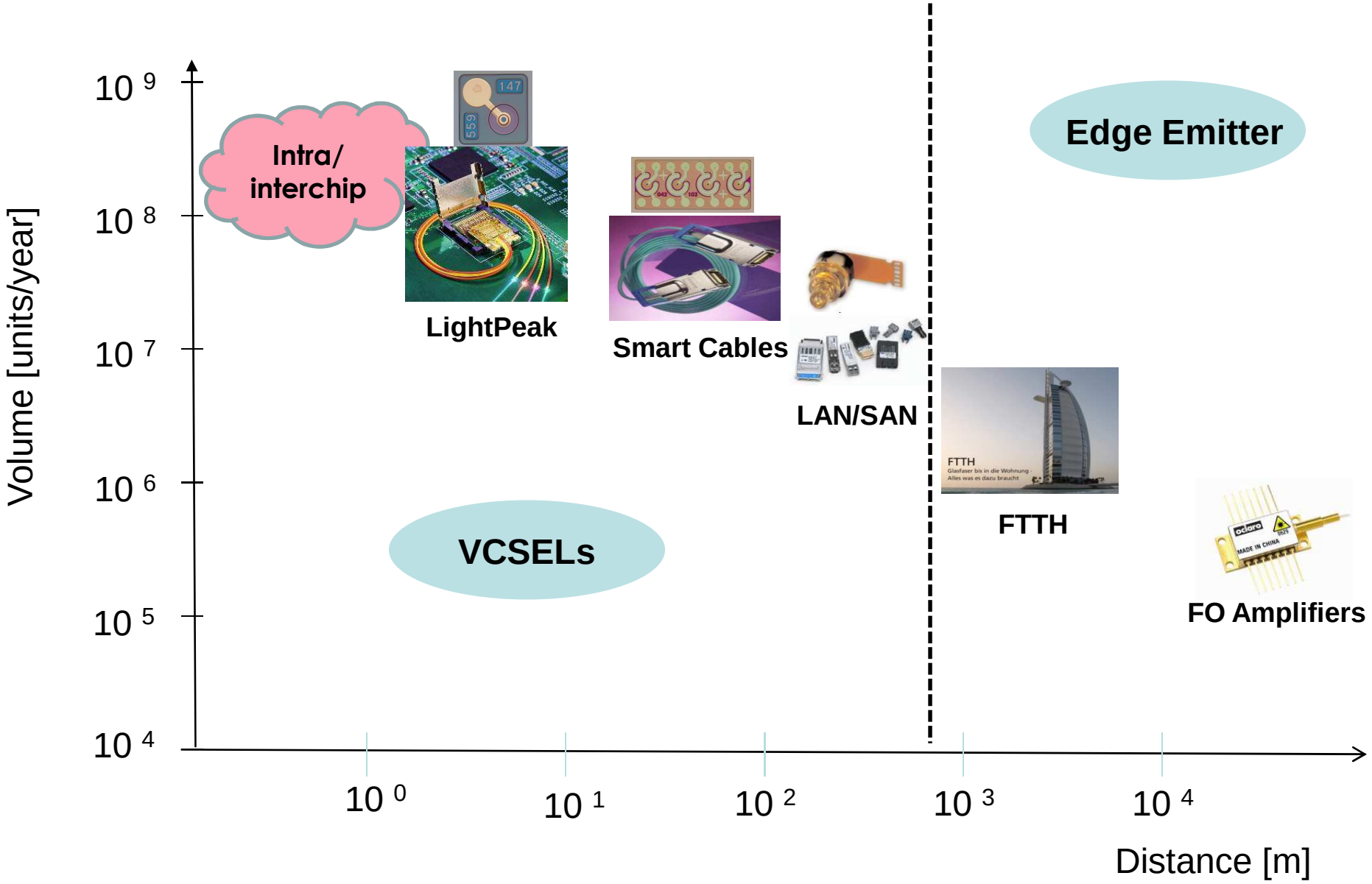
- Vertical Emission
- On Wafer testing
- Simple Assembly
- Small (80'000/3"Wafer)
- High Reliability and high modulation speed
- Symmetric beam
- Most efficient conversion electrical to optical power (~1 mW)
- 2D arrays optional
- Wavelength range 680 nm – 2‘000 nm







Optical Datacom and O/I-Markets



Other VCSEL Markets

- Computer mouse
- Finger navigation
- Encoder
- Gas Sensing
- Atomic Clocks
- FT-Spectroscopy
- Illumination

Consumer: Large volumes (100M+)
Industrial: Single mode & polarization stable

1999 Technology Roadmap

Table 6 - Projected performance of 2D InGaAs VCSEL and driver arrays (980 nm)

Year	1997 *(a)*	1999 *(b)*	2002	2007
Optical channels	256 (16 x 16)	256 (16 x 16)	1024 (32 x 32)	4096 (64 x 64)
Chip size (mm^2)	2.5 x 2.5	2.5 x 2.5	3.2 x 3.2	4.0 x 4.0
Pitch (VCSEL + driver) (µm)	125 (250)	125 (250)	100	System dependent, envisage 62.5
VCSEL active diameter (µm)	15	10	4	2
Bit rate per channel (Gbit/s)	0.6	1.2	4	8
Aggregate bit rate (Gbit/s)	10 154 *(c)*	80 320 *(d)*	1000	33000
Modal properties	multi-mode	multi-mode	single mode	single mode
Operating voltage (V)	2.5 *(e)*	2.5	2.0	1.8
Threshold current (mA)	3	1	0.5	0.1
Operating current (mA)	6	6	1.5	0.5 *(f)*
Optical output power (mW)	1	2	0.5	0.3
Power dissipation - individual VCSEL (mW) - VCSEL array (W) – VCSEL driver array (W) (@ 50 % duty cycle) *(g)*	 14 1.8 + 0.7 3.8 *(h)* + 1.4	 11 1.4 + 0.2 1.5	 2.5 1.3 + 0.4 5	 0.6 1.2 + 0.3 7 *(i)*
Signal delay (ns) Driver to optical output	0.8	0.5	0.15	0.08
Uniformity Threshold current ± (%) output power ± (%) delay + (ns)	 10 20 0.4	 10 20 0.4	 5 10 0.1	 5 10 < 0.06
Yield within array (%)	99%	99%	99.9%	99.9%

See appendix for remarks.

Technology Roadmap, European Comission,
Advanced research initiative in microelectronics MEL-ARI OPTO, 2nd edition, Sept. 1999

European Comission **1999** projections for VCSEL arrays for **2007**:

- 2D VCSEL arrays
- Bottom Emission
- Aggregate Bit Rate 33 Tbit/s
- Single Mode
- Operating current/VCSEL ~ 0.5 mA
- Power consumption/VCSEL ~ 0.6 mW

Target Applications:
Intra- and inter-chip interconnects

2010: Intra-chip and inter-chip interconnects still electrical

Electrical vs. optical interconnects

Electrical

Fundamental limit *

B ~10^6 A/l^2 Gbit/s

Example: A = 1 cm^2

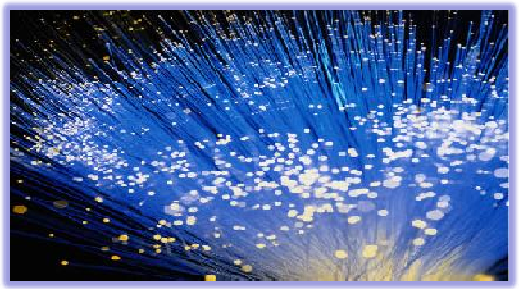
l = 1000 cm

B ~ 1 Gbit/s

HDTV Signal: 1920 x 1080

~ 2 Gbit/s

Optical

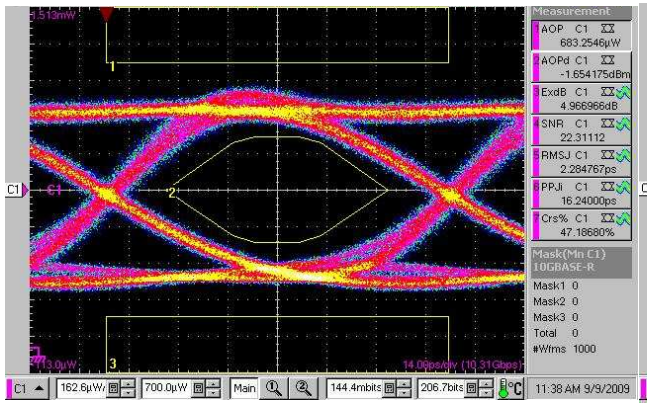


No comparable scaling limits

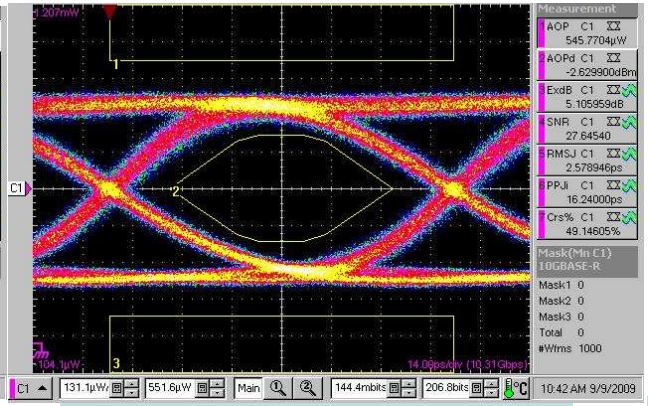
** See: D. A. B. Miller, "Physical Reasons for Optical Interconnection," Special Issue on Smart Pixels, Int'l J. Optoelectronics **11** (3), 155-168 (1997)*

10.3 Gb/s VCSEL TOSA

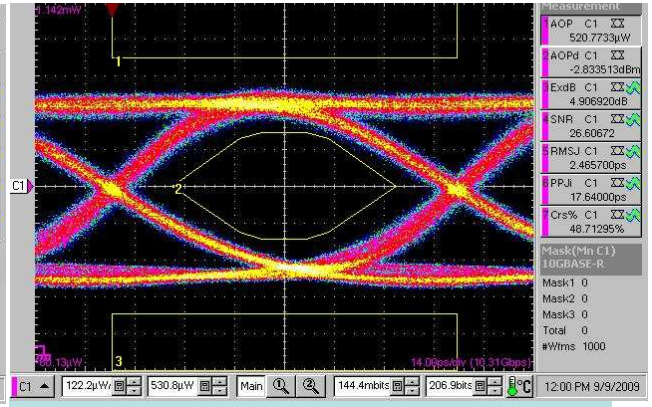
Tektronix scope DSA8200 (plug-in 80C08C)
Vitesse 7985 VCSEL driver



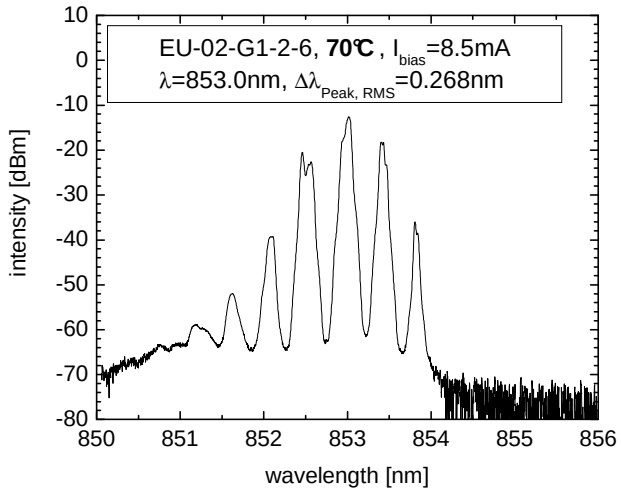
T=-20 C, I_{bias}~ 6mA, ER=5dB
30% Margin



T=25 C, I_{bias}~ 6mA, ER=5dB
30% Margin



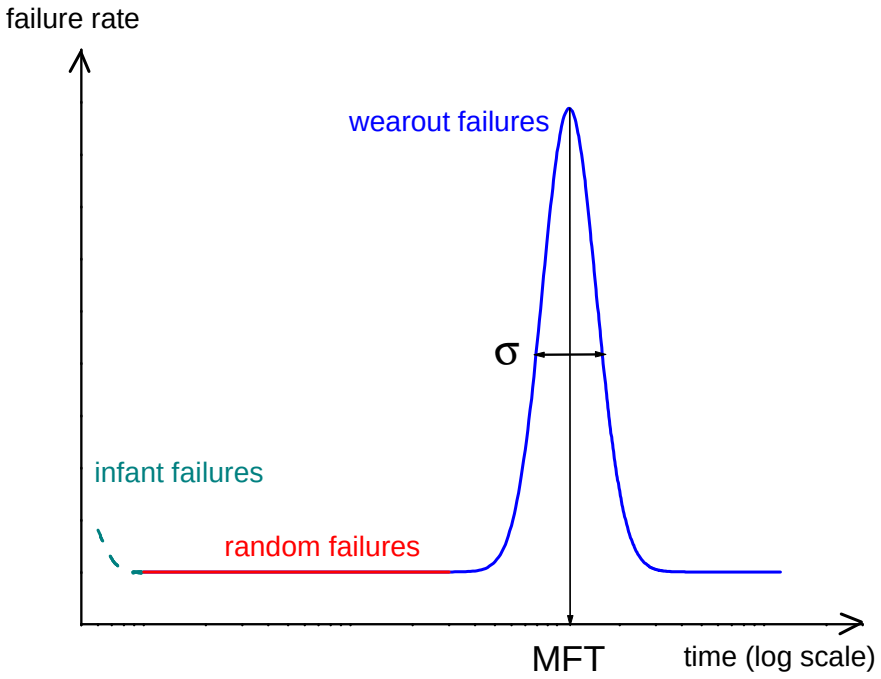
T=85 C, I_{bias}~ 8.5mA, ER=5dB
30% Margin



- Good temperature stability
- Large mask margins @ 10.3 Gb/s
- Narrow linewidth (< 0.3 nm)

Application: Gigabit Ethernet

VCSEL Reliability requirements



Optical interconnects:

- MFT > 30 years @ 70C
- Random failure rate < 100 ppm over product lifetime
- Negligble infant failure rate

Random failure Rate

- 10G VCSEL: 1‘637 VCSELs from 10 wafers

  ⇒ No failure

- Similar VCSEL: 14‘467 VCSELs from 96 wafers

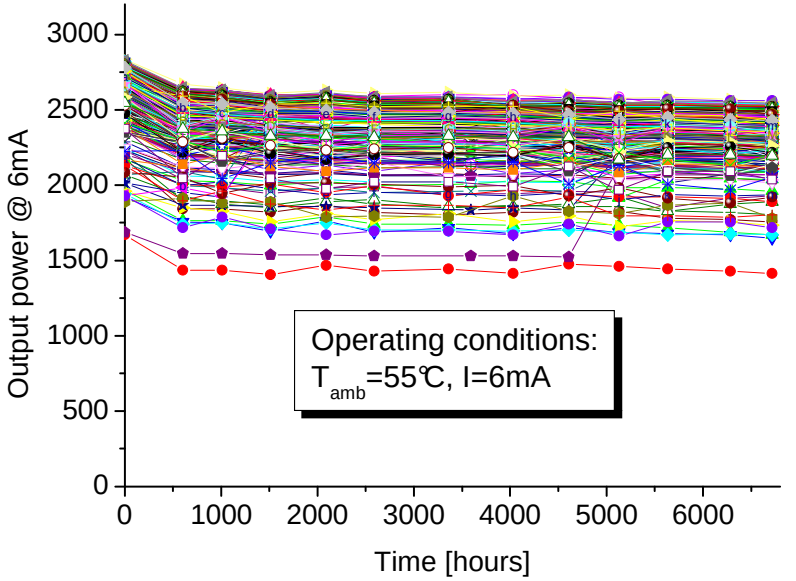
  ⇒ No failure

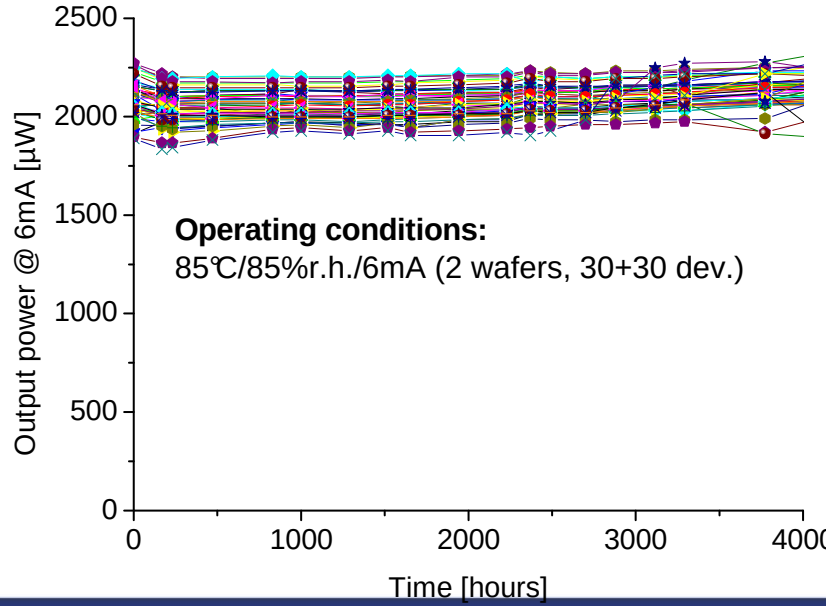
Ambient temperature	ppm levels over 1 year
25℃	< 57
40℃	< 103
55℃	< 176

Additional reliability tests

- VCSEL chips
- Consumer applications

- Biased 85 /85
- Low temperature (-40C)
- Damp heat cycles
- Thermal shocks (-40, 25, 125C)
- Mixed gas



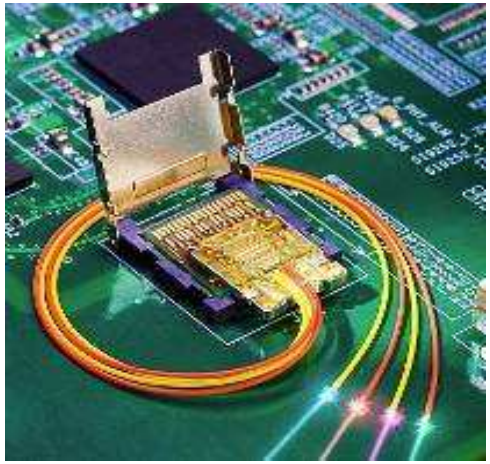


High volume VCSEL manufacturing

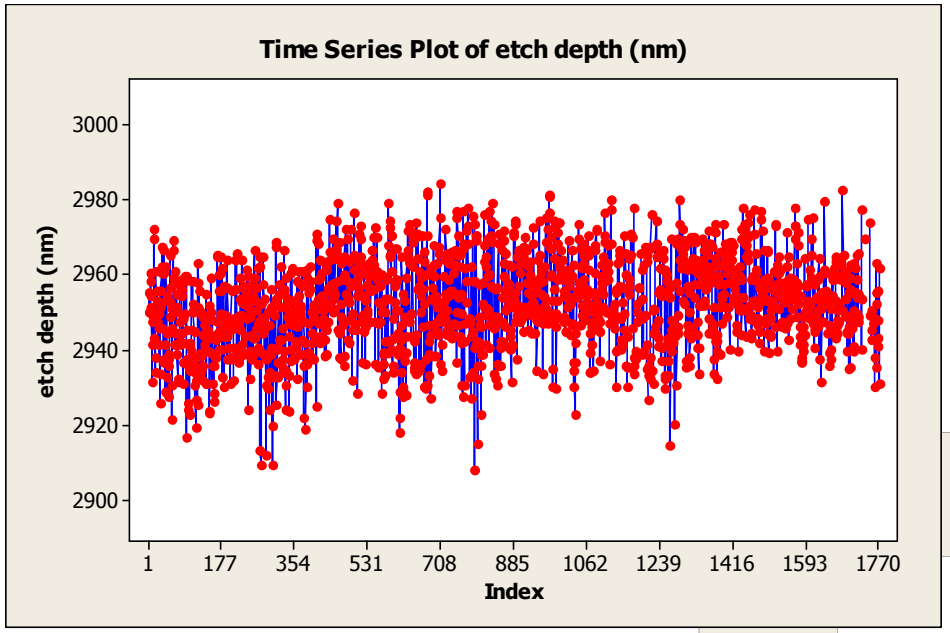
- Each week ~ 600 addtl. VCSELs on reliability test

  ⇨ Efficient reliability testing procedures

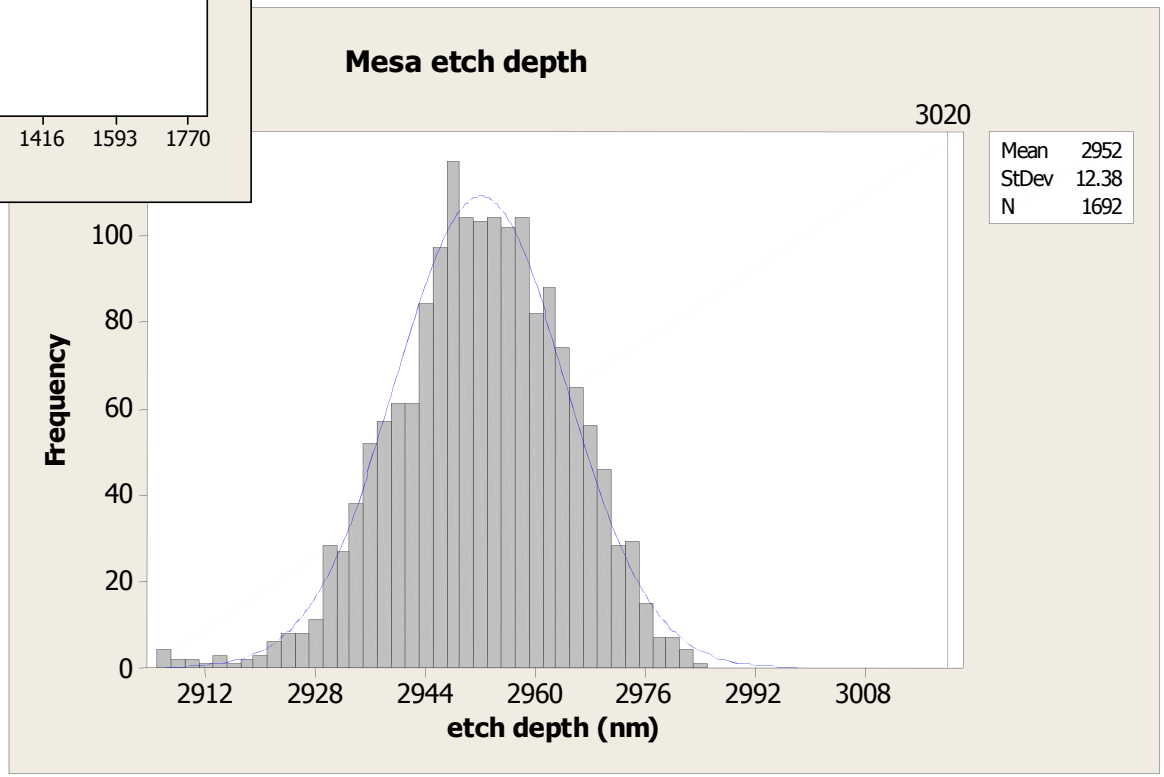
- Strict SPC Control required
  - Many in-line controls
- Continuous cost reduction
  - Smaller die size
  - Efficient processes
  - Testing capabilities



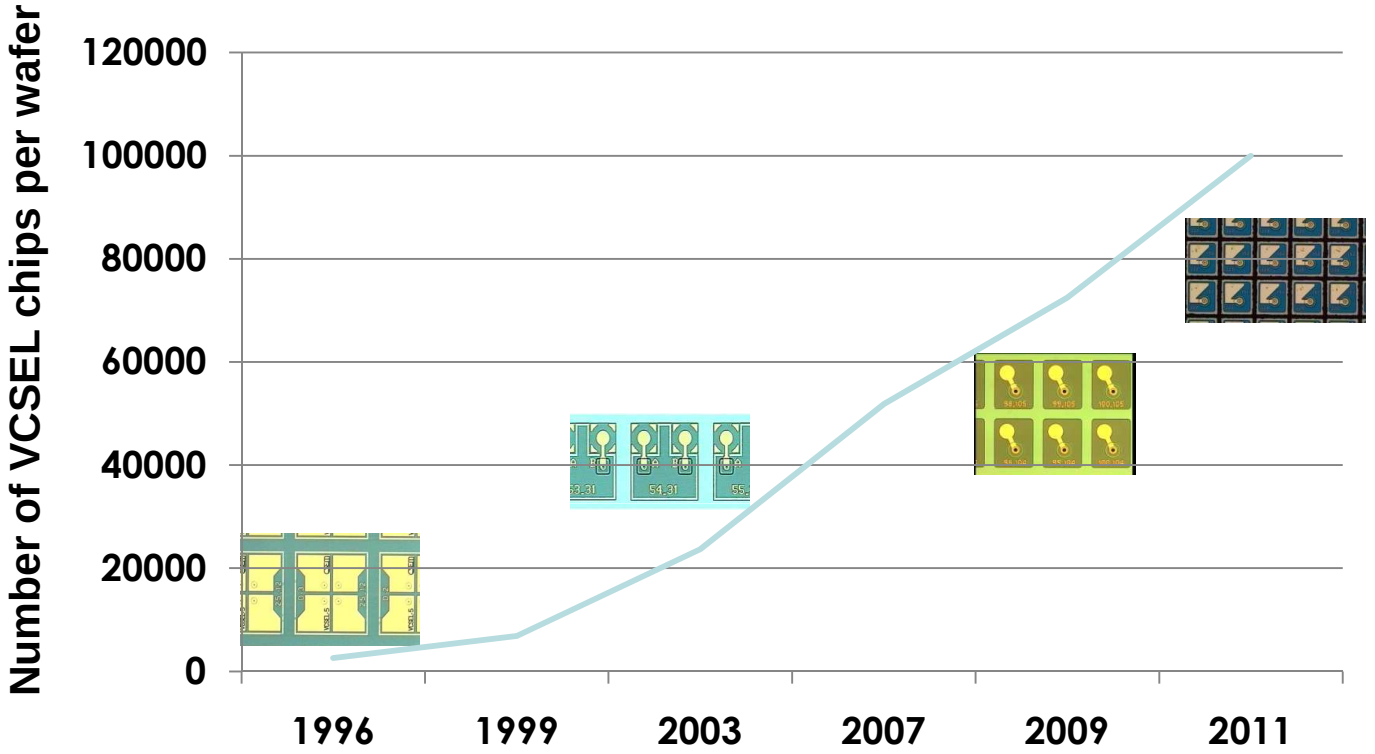
Mesa etch depth



Target etch depth: 2950nm
Data of >1600 wafers



Cost reduction



Tenfold increase in number of VCSELs per wafer over the last 10 years
Trend to continue in the coming years

Summary

VCSELs for optical interconnects:

- Modulation speed > 10 Gbit/s now (25Gbit/s)
- Very low FIT rates, high reliability
- High volume manufacturing capability (100M+/year)
- Cost efficient manufacturing
  - More devices / wafer (Dicing)
  - Bigger Wafers (uniformity)
  - Efficient processes
  - Testing Capabilites
- Process control
  - Many in line controls
  - 6 Sigma tools